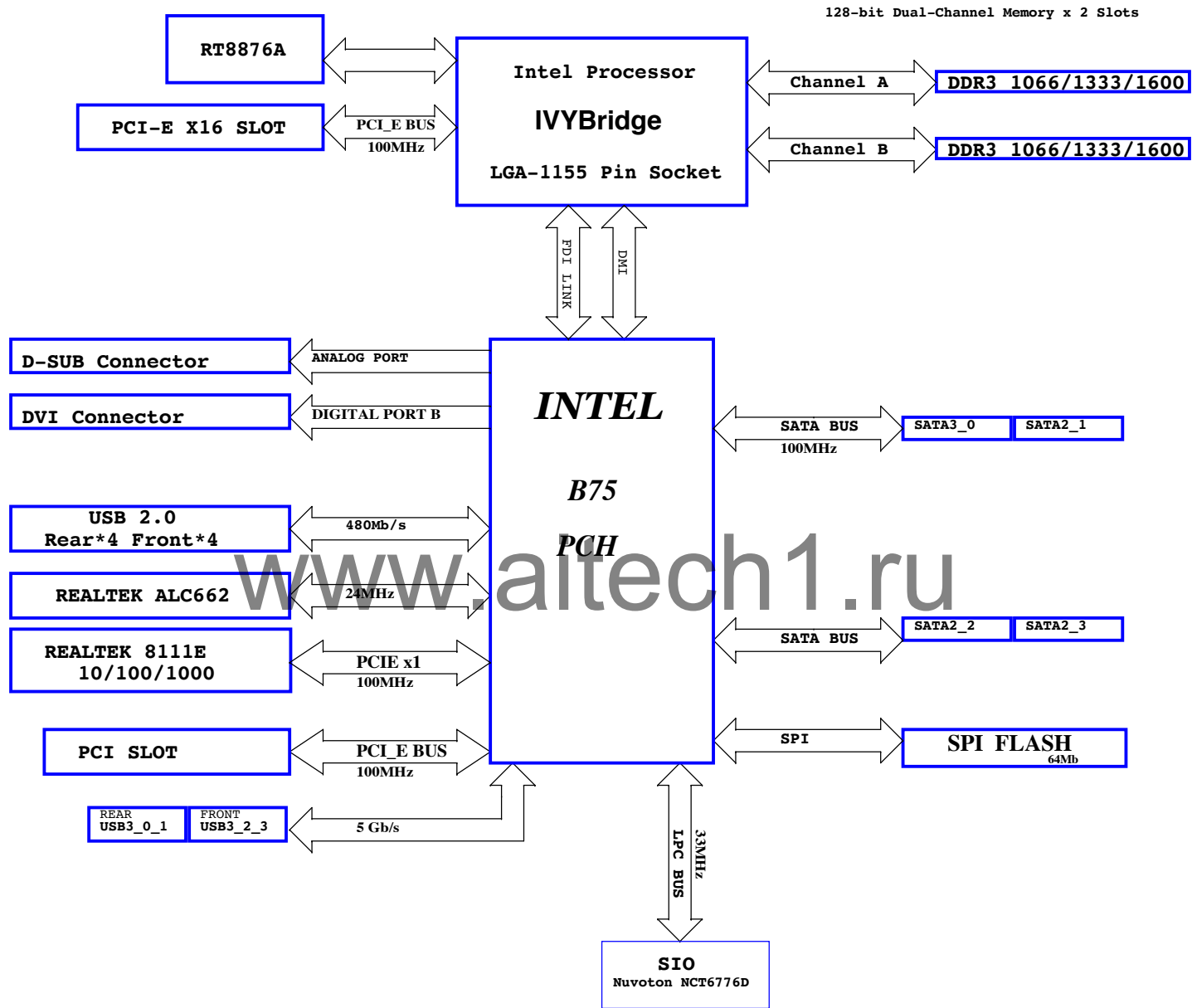
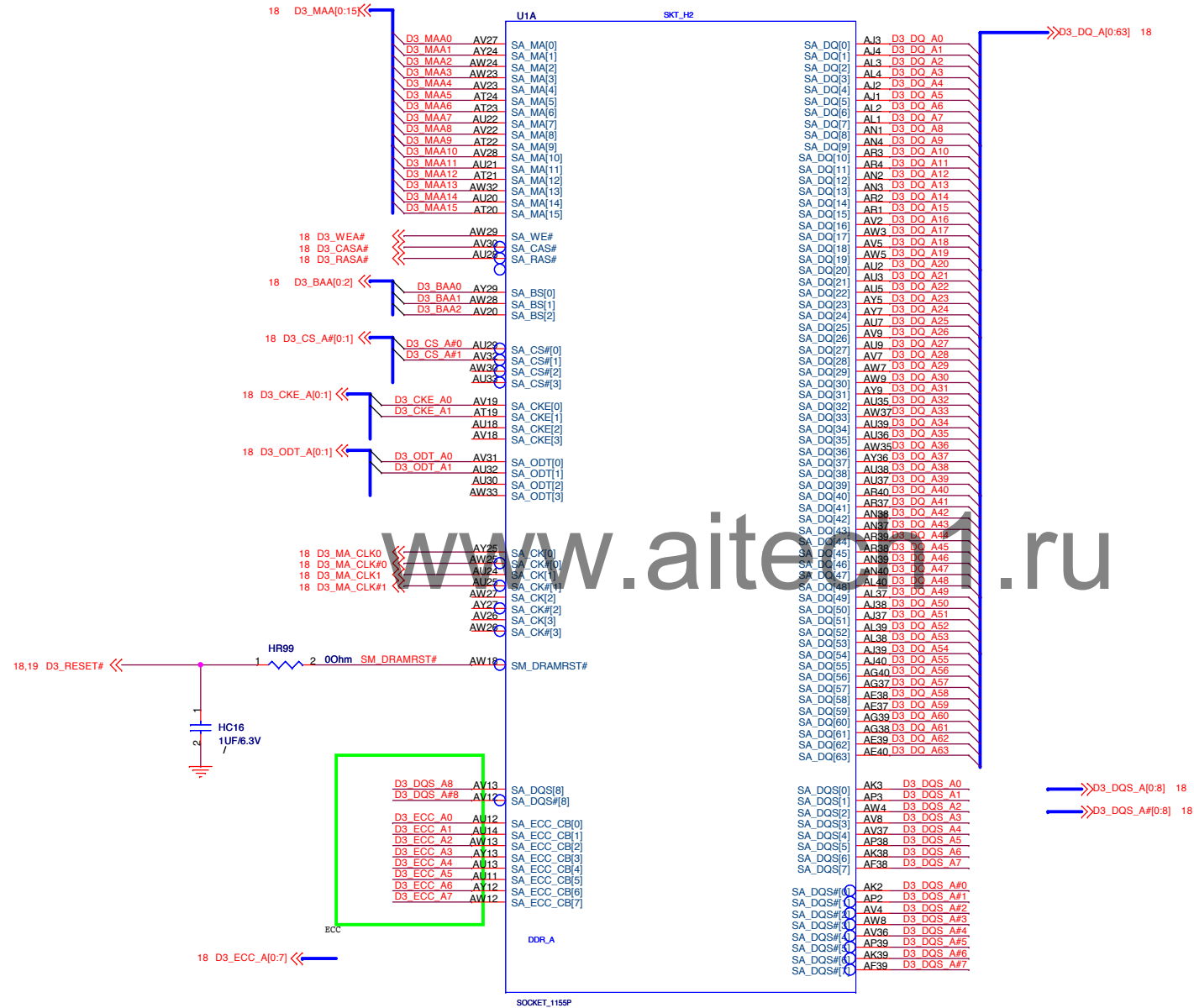


B75M-DGS R2.00

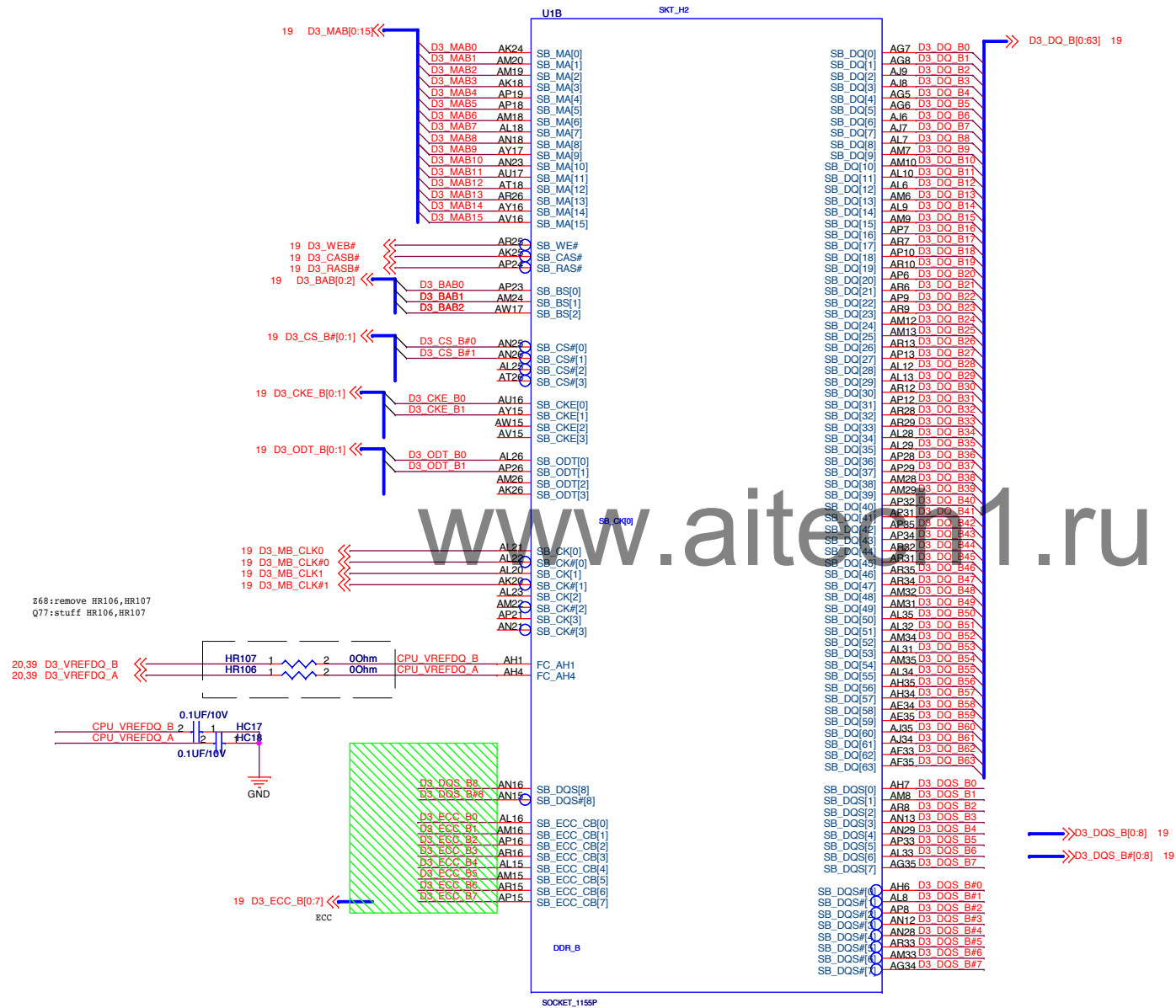


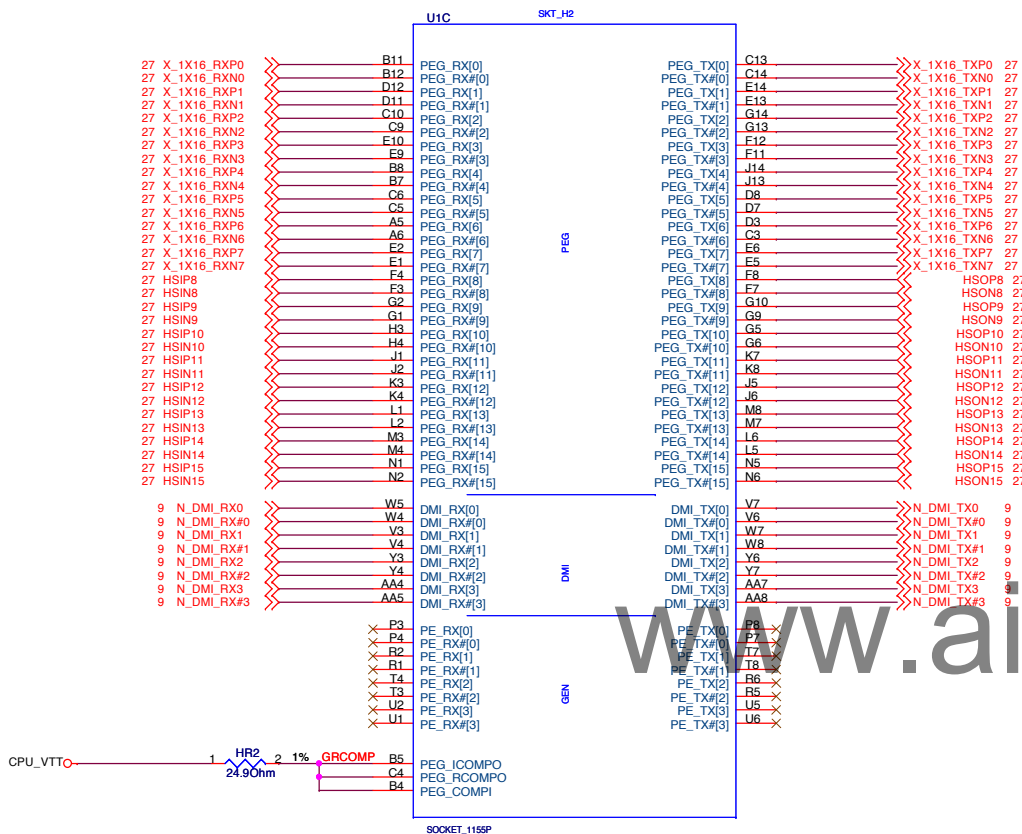
NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



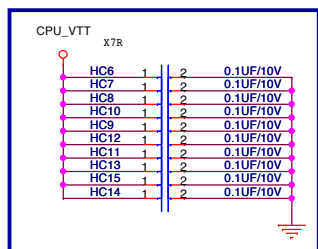
B75M-DGS

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!





GRCOMP<500mil
U1.B4 and U1.C4 tight together then use 4 mil trace to HR2.2
U1.B5 use 10 mil trace separate to HR2.2



for PCIE signal trans-layer decoupling capacitors!!!
Place near trans-layer vias for PCIE lanes.

B75M-DGS

can not connect to clock gen. must be provided by PCH.

2000 mil <U1.AJ19 to HR45 <3000 mil

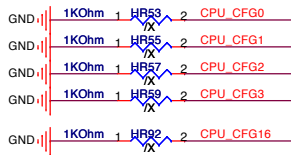
For future processor compatibility, the PROC_SEL should be connect to the NV_CLE pin on the PCH through an isolation resistor of 4.7K ohm and a 2.2k ohm pull up to V_NAND_IO (+1.8V).

Reserved for testing purpose:

Must have: CFG[3:0], CFG[16] test points.

Nice to have: CFG[7:0], CFG[16] test points.

Very nice to have: Nice to have: CFG[15:0], CFG[16] test points.



14 PCH_CK_DMI#
14 PCH_CK_DMI#

11 CPU_PWRGD
VCCM

10 PM_SYNC

45 PROCHOT#
10 H_THERMTRIP_N

17 H_SKTOCC#
16 PROC_SEL

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

17 H_SKTOCC#

www.aitech1.ru

U1E SKT_H2

CPU_CFG0 H36
CPU_CFG1 J36
CPU_CFG2 J37
CPU_CFG3 K36
L36
N35
L37
M36
J38
L35
N38
N38
N39
N37
N40
G37
G36

AT14
AY3
H7
H8

BCLK[0]
BCLK[0]
VIDCLK
VIDOUT
VIDALERT#

UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

PM_SYNC
PECI
CATERR#
PROCHOT#
THERMTRIP#

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

SKTOCC#
PROC_SEL
SM_VREF

RSVD28
VCCSA_VID
VCCSA_SENSE

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

VCCAXG_SENSE
VSSAXG_SENSE

TDO
TDI
TCK
TMS

TRST#
PRDY#
PREQ#
DBR#

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

RSVD28
VCCSA_VID
VCCSA_SENSE

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

VCCAXG_SENSE
VSSAXG_SENSE

TDO
TDI
TCK
TMS

TRST#
PRDY#
PREQ#
DBR#

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

RSVD28
VCCSA_VID
VCCSA_SENSE

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

VCCAXG_SENSE
VSSAXG_SENSE

TDO
TDI
TCK
TMS

TRST#
PRDY#
PREQ#
DBR#

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

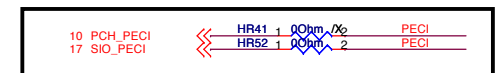
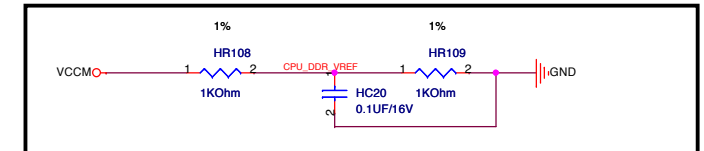
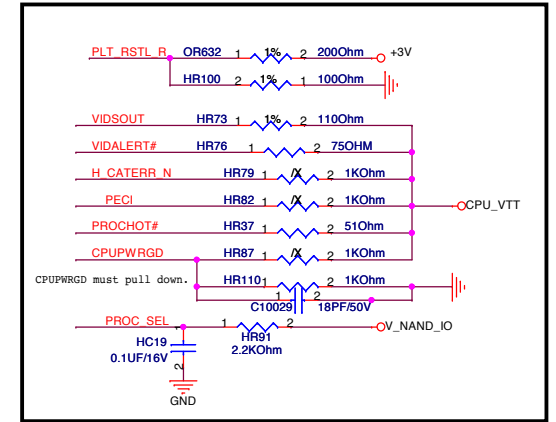
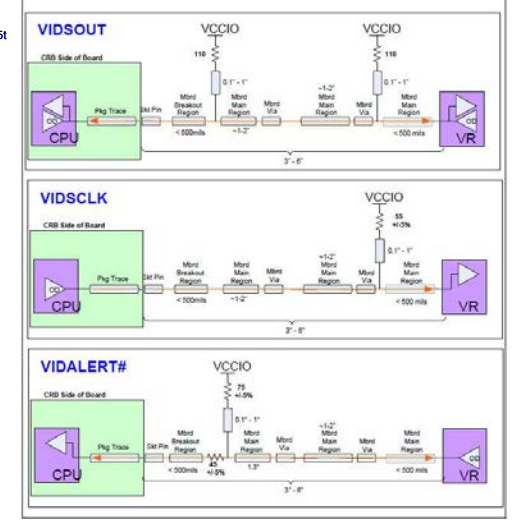
VCC_NCTF
RSVD40

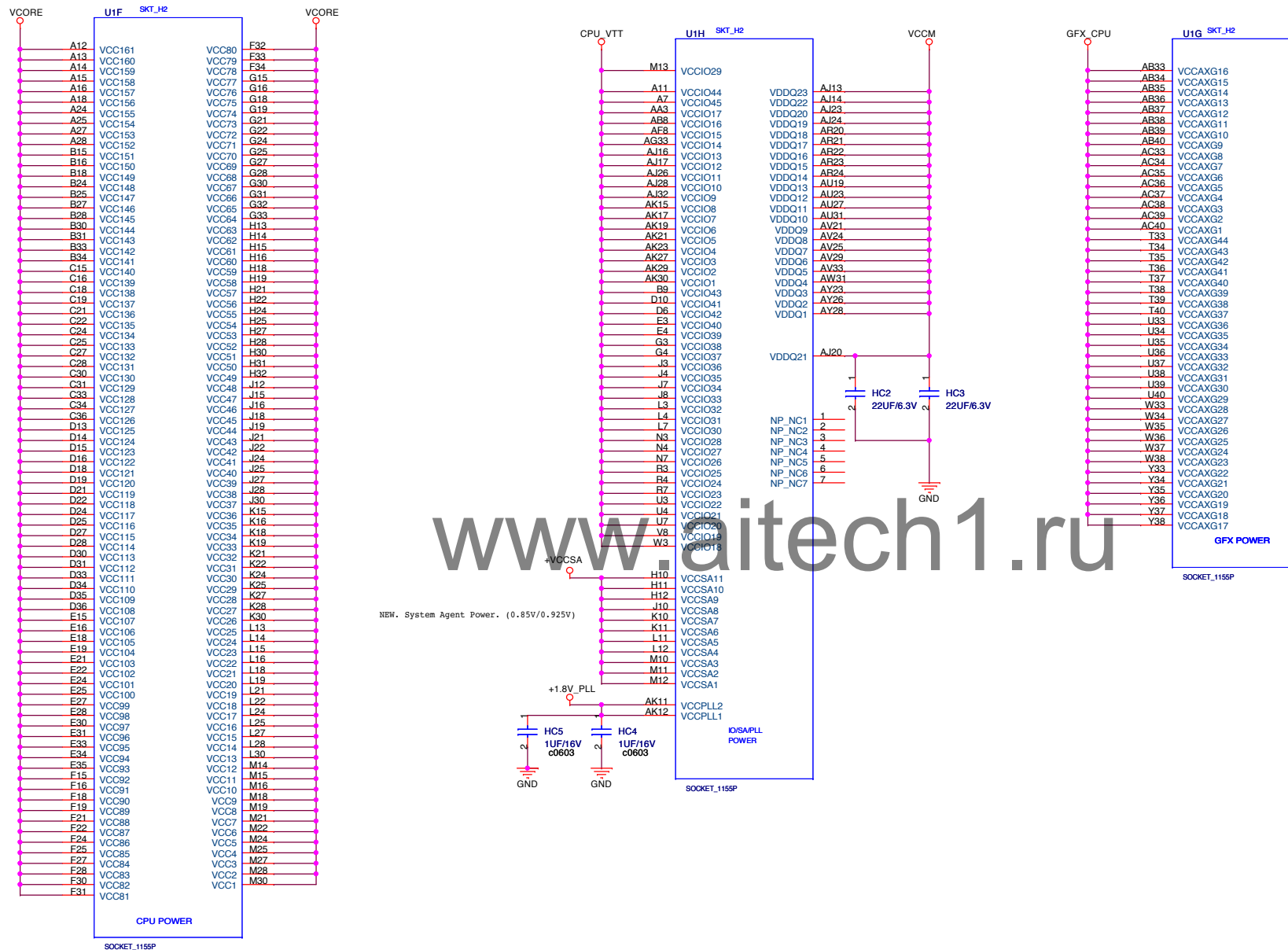
VCC_NCTF
RSVD40

VCC_NCTF
RSVD40

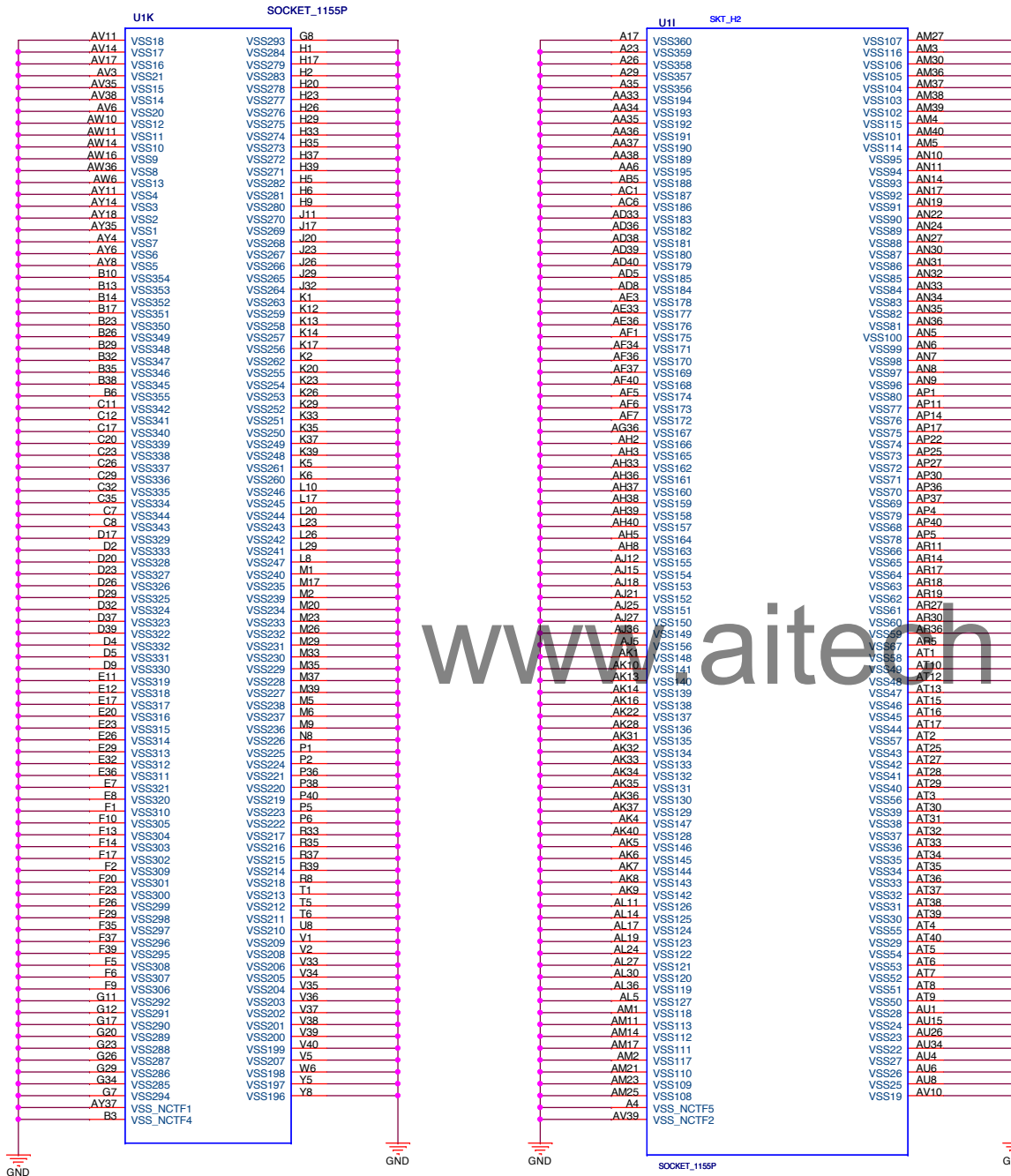
VCC_NCTF
RSVD40

SVID Placement needs to pay attention for pull up resistors. See PDG page 330

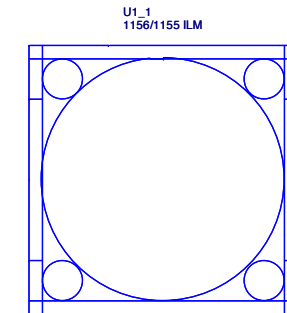
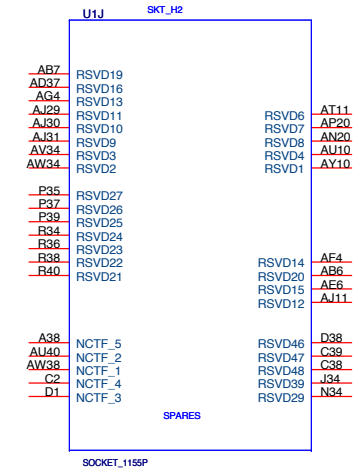




B75M-DGS



All reserved. No connected.



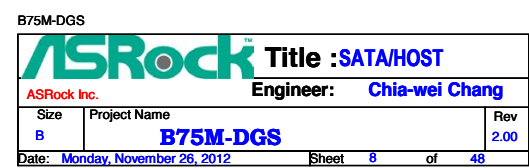
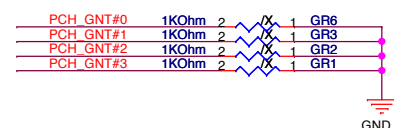
B75M-DGS

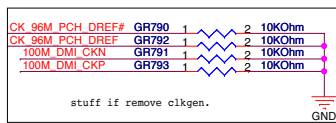
ASRock Title : CPU - GND		
ASRock Inc. Engineer: Chia-wei Chang		
Size	Project Name	Rev
A3	B75M-DGS	2.00
Date: Thursday, November 22, 2012		Sheet 7 of 48

PCI

Phantom

www.aitech1.ru





PCie Port 1 need to connect to Slot.
Do NOT connect to IC.

LAN1 (x1)

www.aitech1.ru

Over Current Pin Default Usage

Pin	Default Port Mapping
OC0#	Port 0, Port 1
OC1#	Port 2, Port 3
OC2#	Port 4, Port 5
OC3#	Port 6, Port 7
OC4#	Port 8, Port 9
OC5#	Port 10, Port 11
OC6#	Port 12, Port 13
OC7#	Not Used

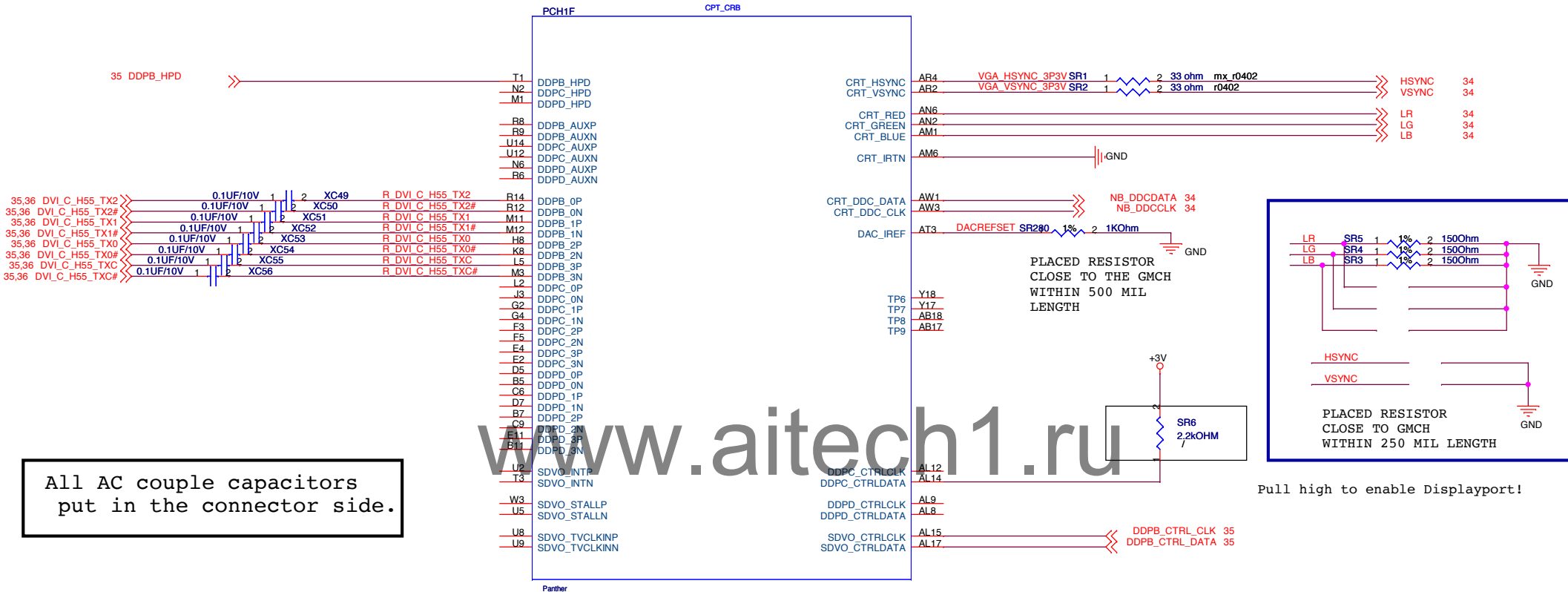
Watch out!!! port 12/13
P/N is different!!

Intel 7 Series chipset USB Port Mapping

USB 2.0 Port Number	USB 3.0 Ports Number
0	1
1	2
2	3
3	4
4	-
5	-
6	-
7	-
8	-
9	-
10	-
11	-
12	-
13	-

B75M-DGS

ASRock		Title : PCIEDMIUSB	
ASRock Inc.		Engineer: Chia-wei Chang	
Size Custom	Project Name B75M-DGS		Rev 2.00
Date: Thursday, November 22, 2012		Sheet 9	of 48



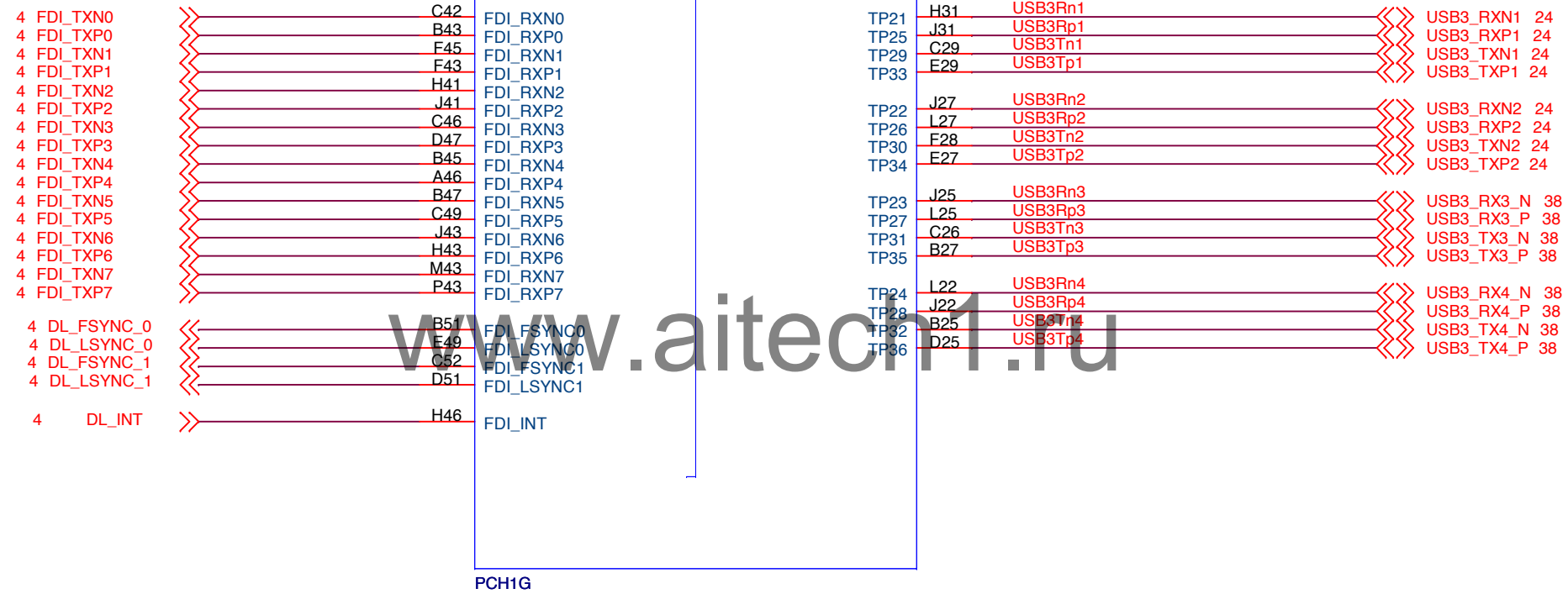
All AC couple capacitors
put in the connector side.

- In an effort to address customer display issues more efficiently Intel recommends customers adopt digital display configuration similar to Intel CRB as following

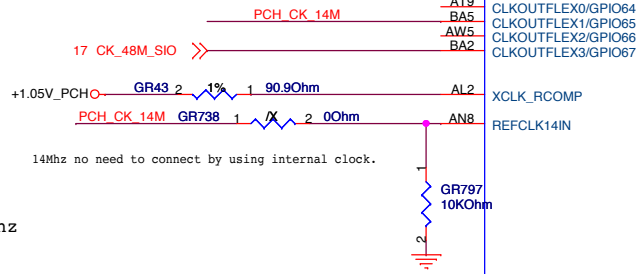
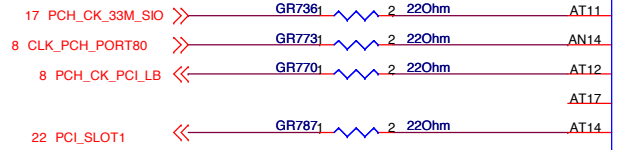
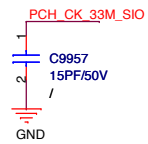
Digital Port	Display Technology
Port B	DVI or SDVO (Desktop) DisplayPort, HDMI/DVI or SDVO (Mobile)
Port C	DisplayPort (Desktop) DisplayPort/HDMI/DVI (Mobile)
Port D	HDMI/DVI/eDP* (Desktop) HDMI/DVI/DisplayPort (Mobile)

B75M-DGS

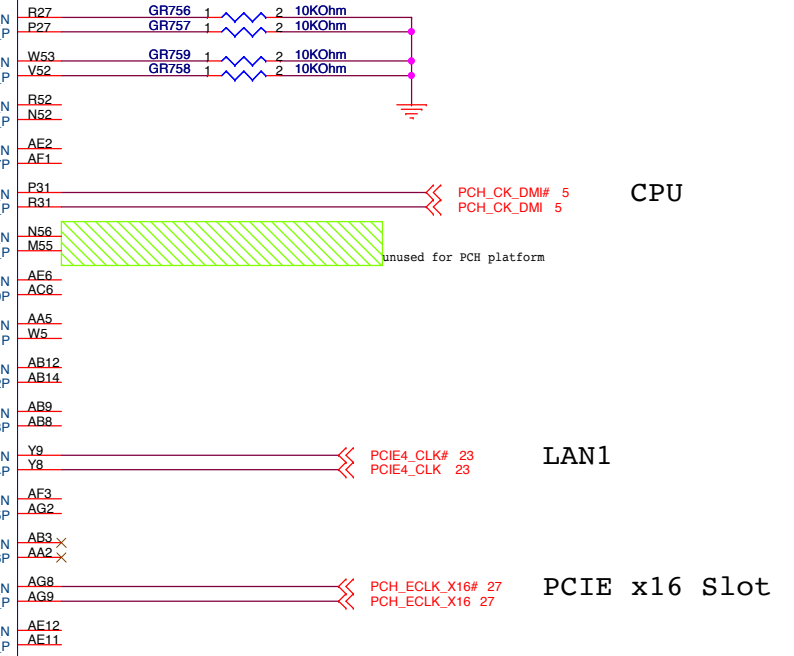
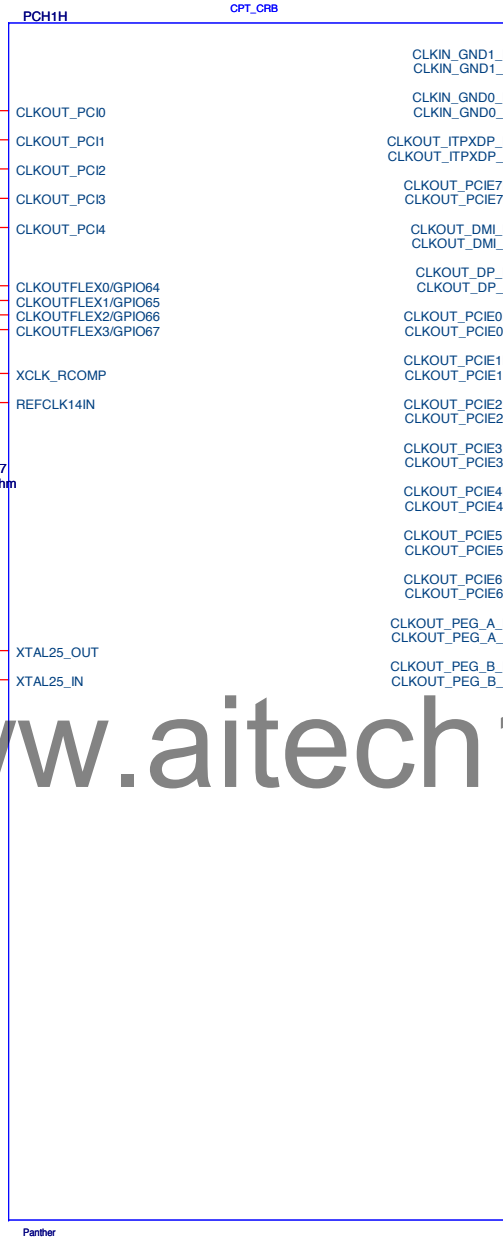
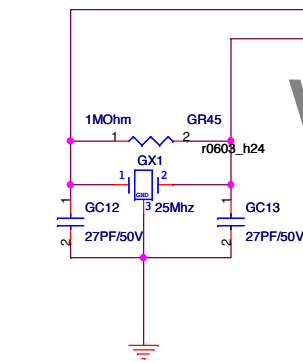
ASRock		Title :Clock Distribution	
ASRock Inc.		Engineer: Chia-wei Chang	
Size B	Project Name B75M-DGS		Rev 2.00
Date: Thursday, November 22, 2012		Sheet 12 of 48	



**FLEX CLK HAS RULE OF USING.
SEE PDG PAGE 191 FOR DETAILS.**



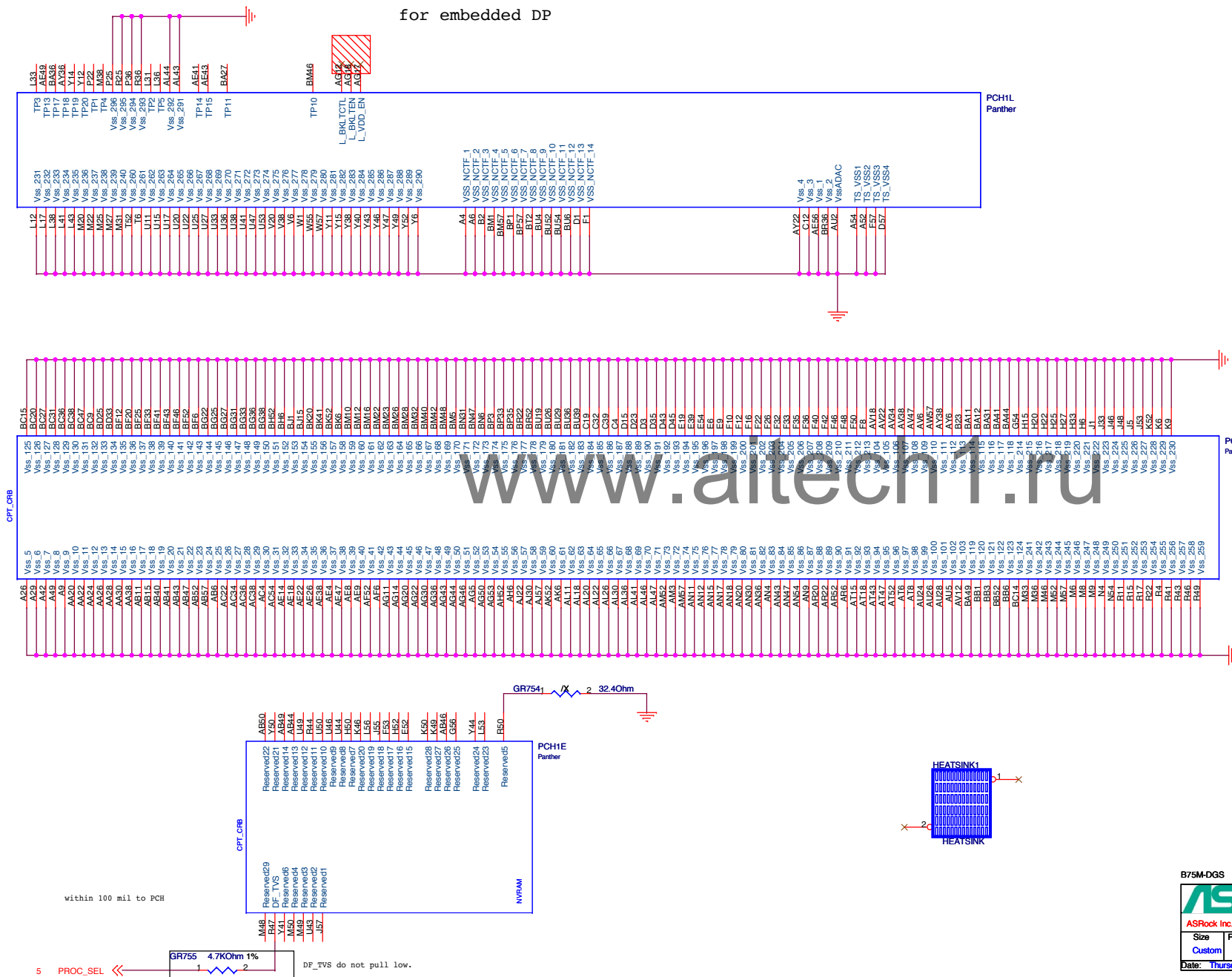
Flex 0, 2 : 33 Mhz
Flex 1, 3 : 27/14/24/48/25 Mhz



www.aitech1.ru

B75M-DGS

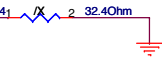
ASRock		Title :CLK	
ASRock Inc.		Engineer: Chia-wei Chang	
Size B	Project Name B75M-DGS		Rev 2.00
Date: Tuesday, November 27, 2012		Sheet 14	of 48



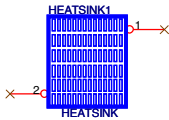
for embedded DP

PCH1L
Panther

PCH1J
Panther



PCH1E
Panther



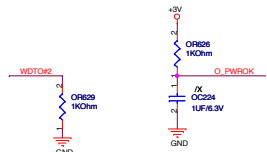
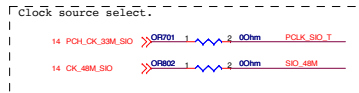
within 100 mil to PCH

DP_FVS do not pull low.

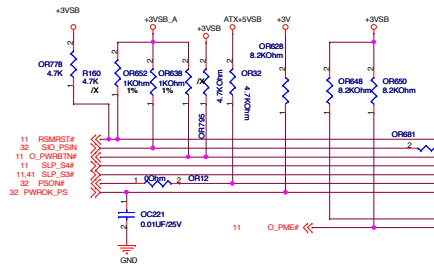
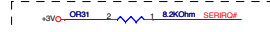
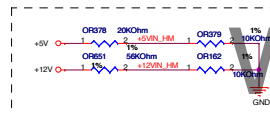
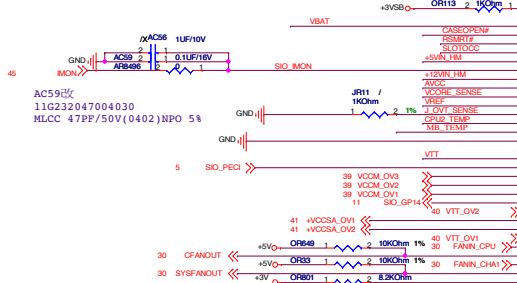
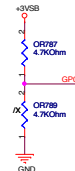
B75M-DGS

ASRock		Title :Panther Point-GND	
ASRock Inc.		Engineer: Chia-wei Chang	
Size	Project Name	Rev	
Custom	B75M-DGS	2.00	
Date: Thursday, November 22, 2012	Sheet 16	of 48	

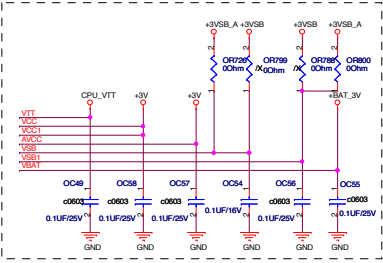
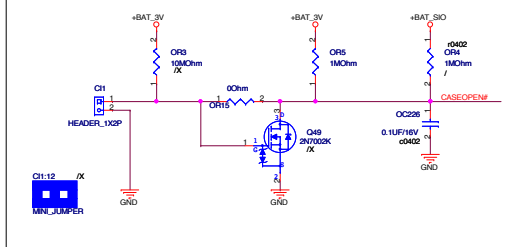
677: SLOTOCC#
667: SLOTOCC



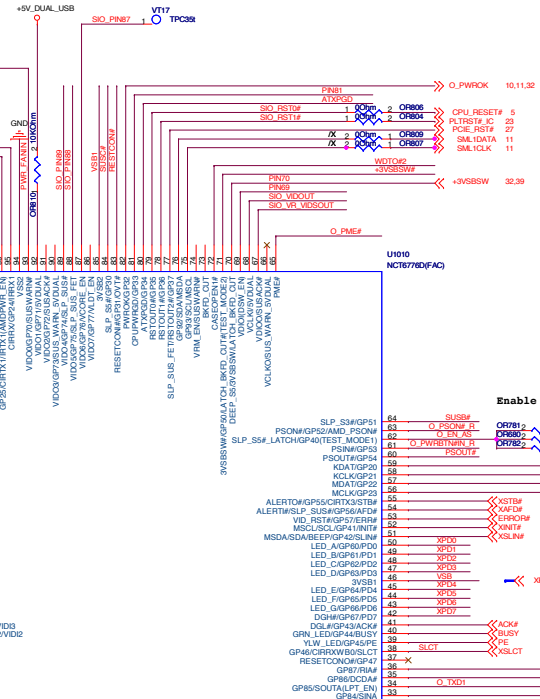
For different version



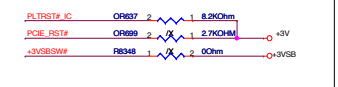
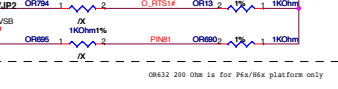
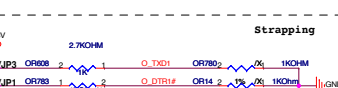
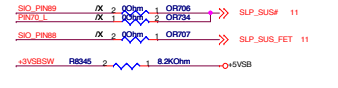
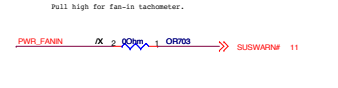
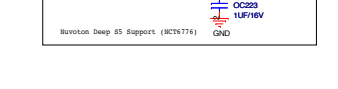
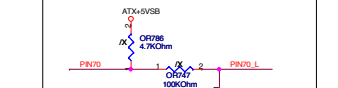
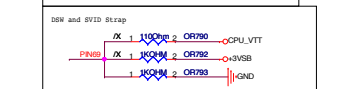
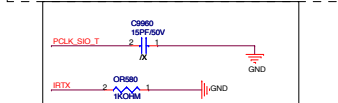
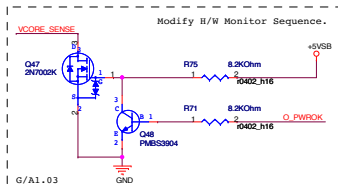
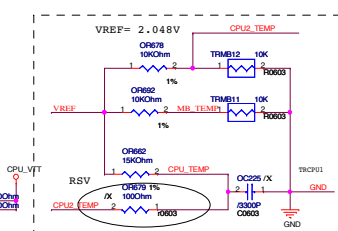
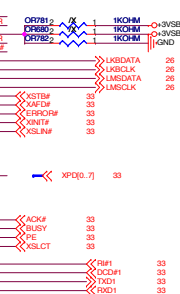
CASEOPEN

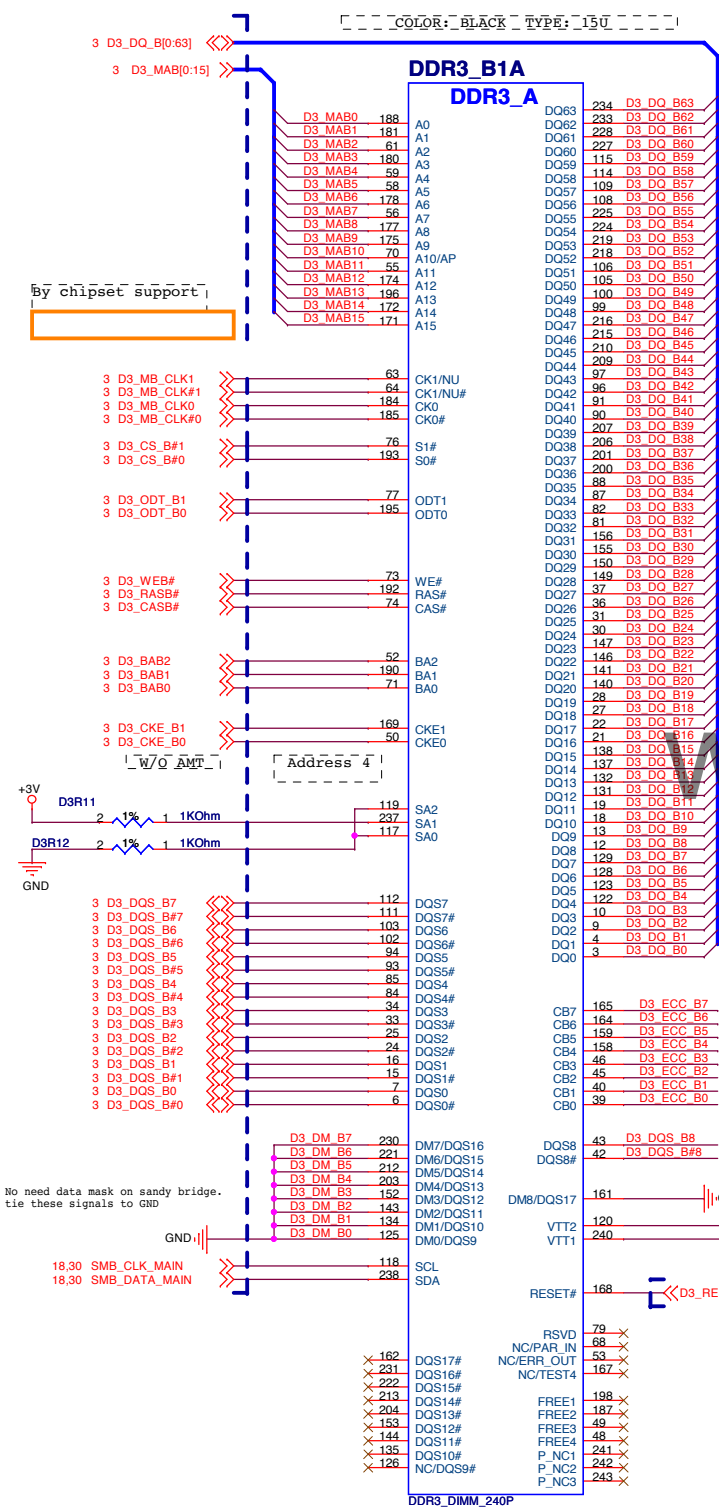


www.aitech1.ru

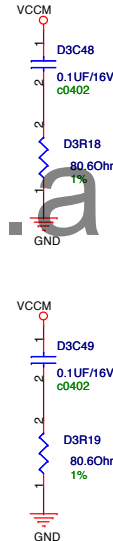


Enable ASUS



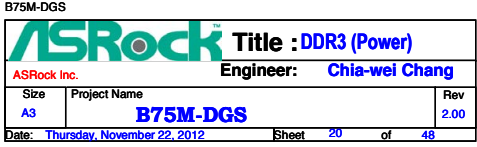


With AMT - w/o AMT
+3V_CL +3V
S0-S5有電 S0有電

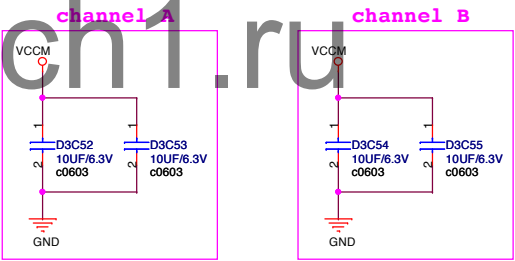


For one channel use.
Delete this block if you
want to design one
channel.

- D3_BAB[0:2] 3
- D3_CS_B#[0:1] 3
- D3_CKE_B[0:1] 3
- D3_ODT_B[0:1] 3
- D3_DQS_B[0:8] 3
- D3_DQS_B#[0:8] 3
- D3_ECC_B[0:7] 3

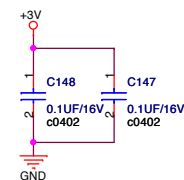
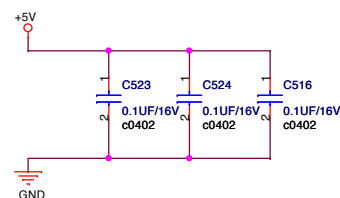


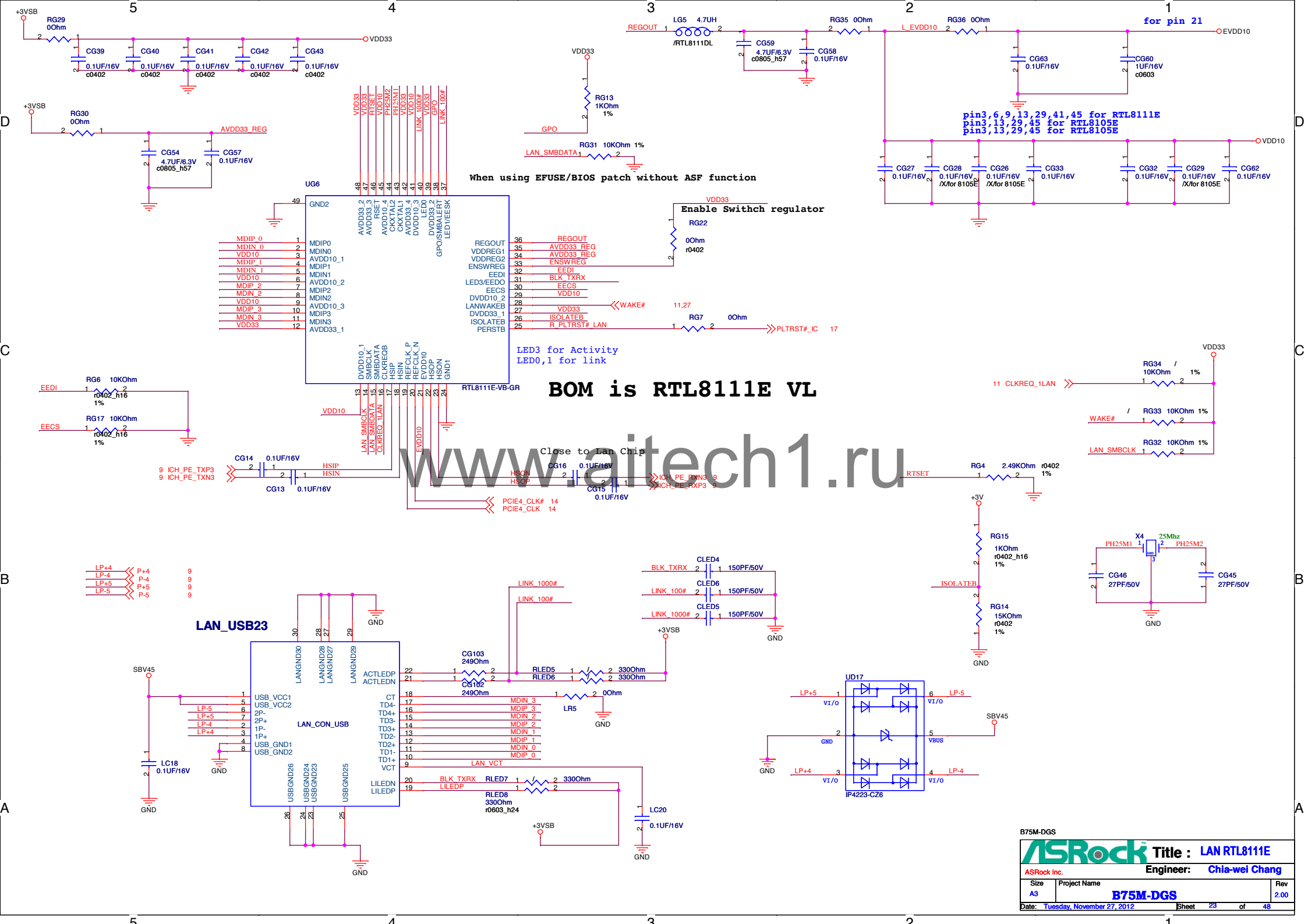
c.w. huang:Add 10uF cap. to improve DDR3 over clock.

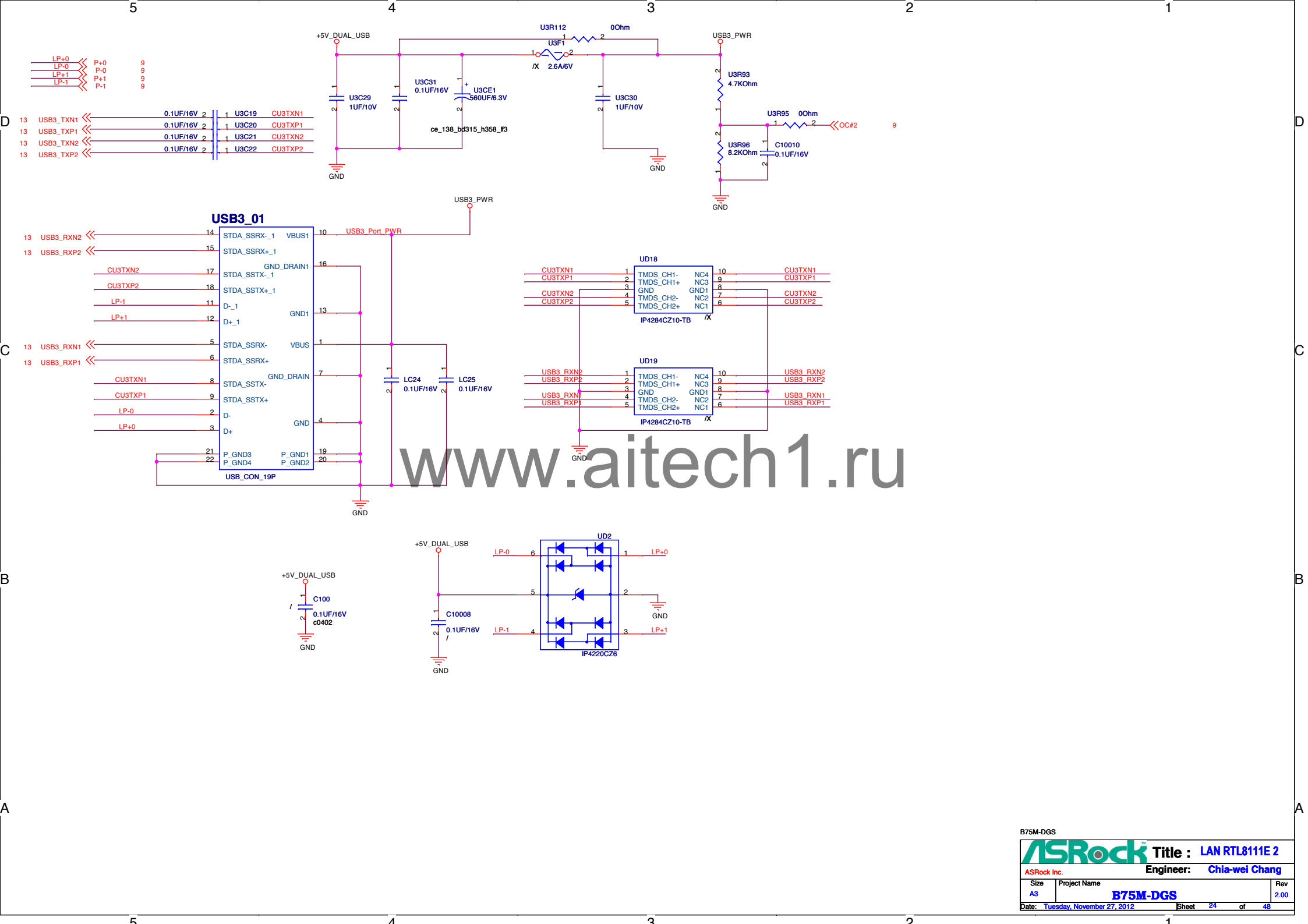




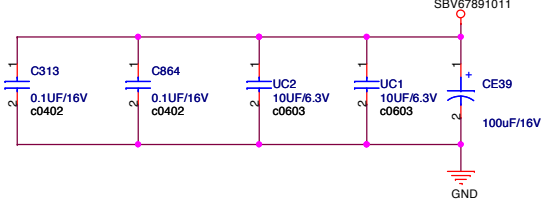
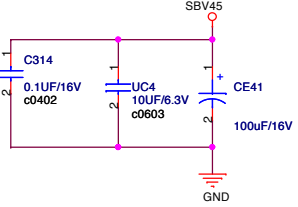
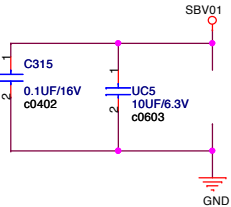
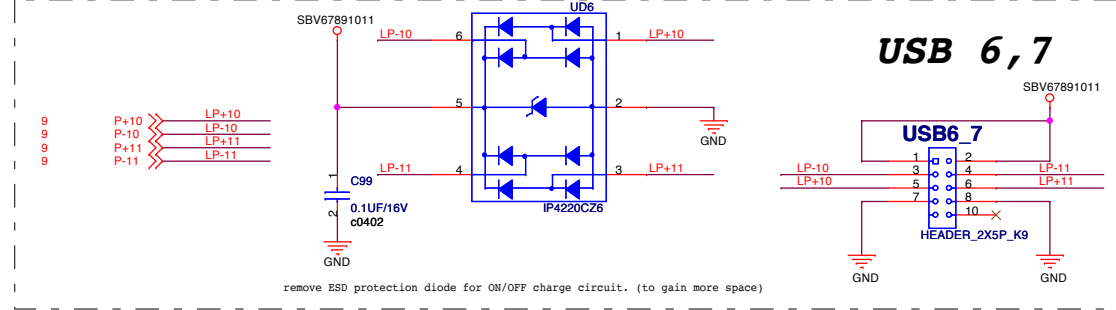
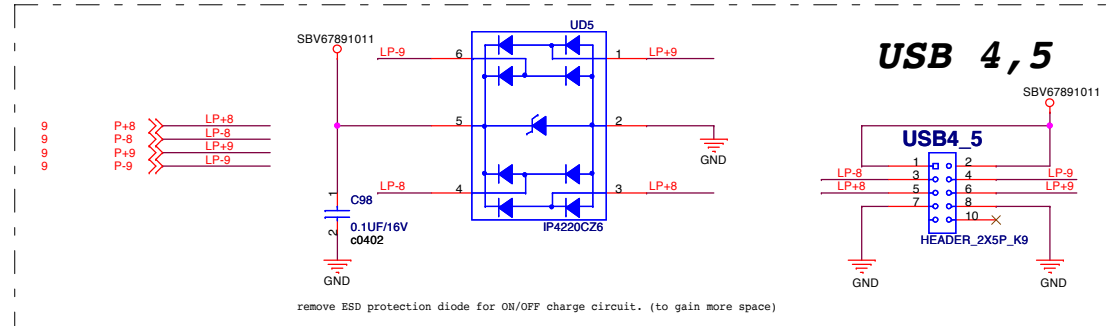
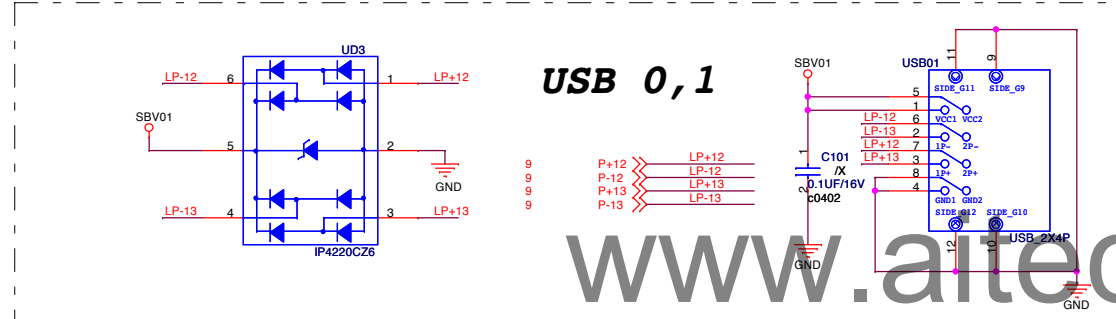
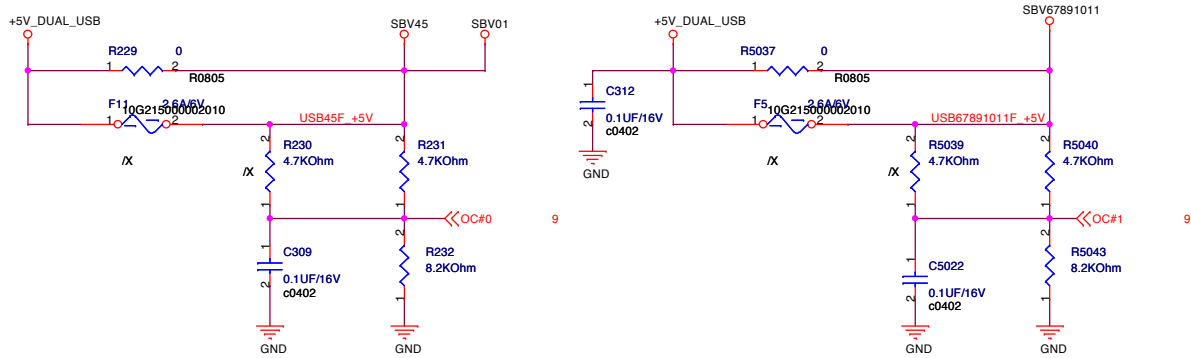
EFGH
IDSEL AD17

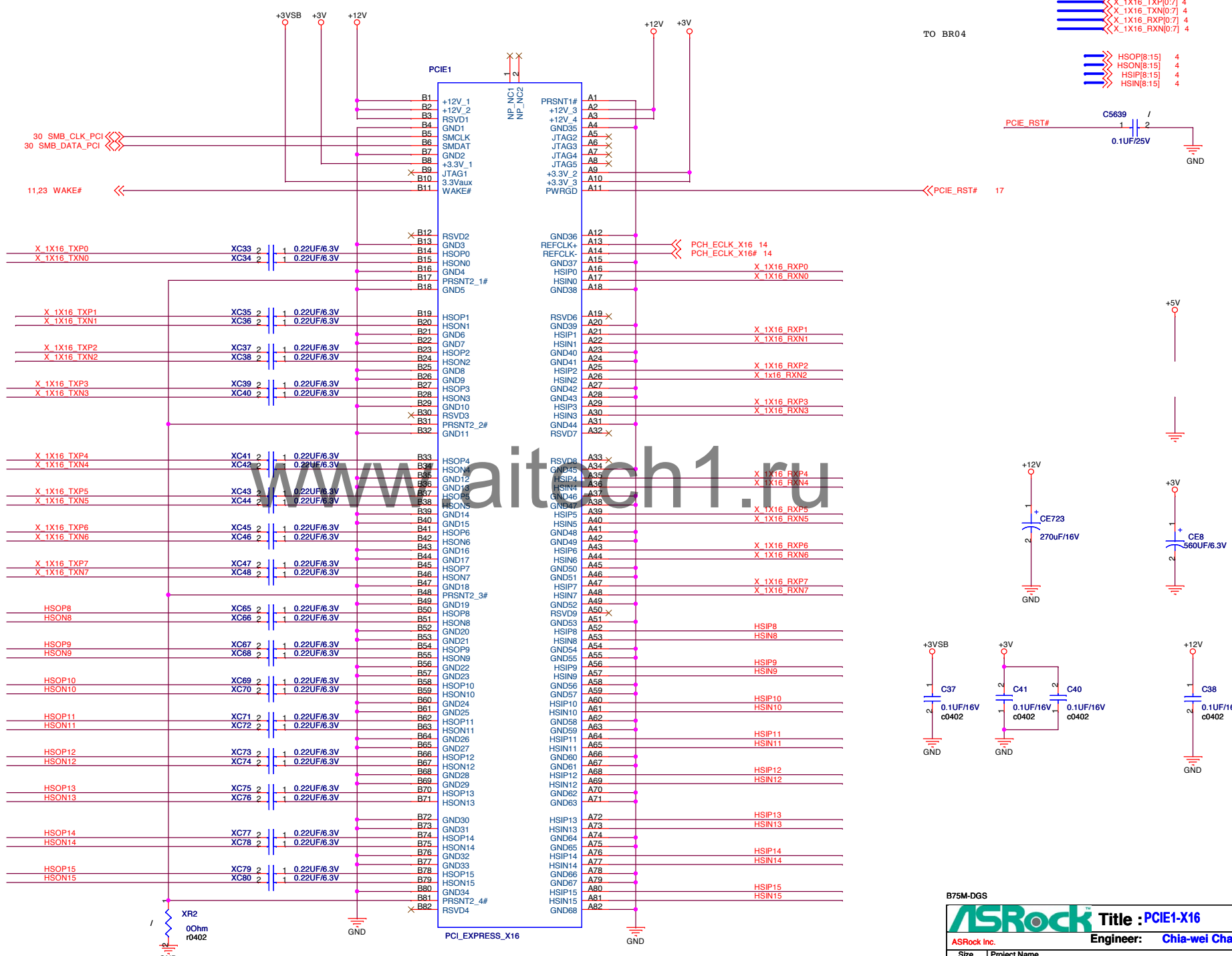


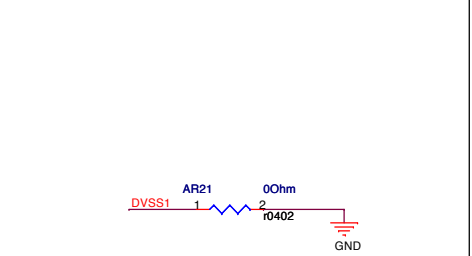
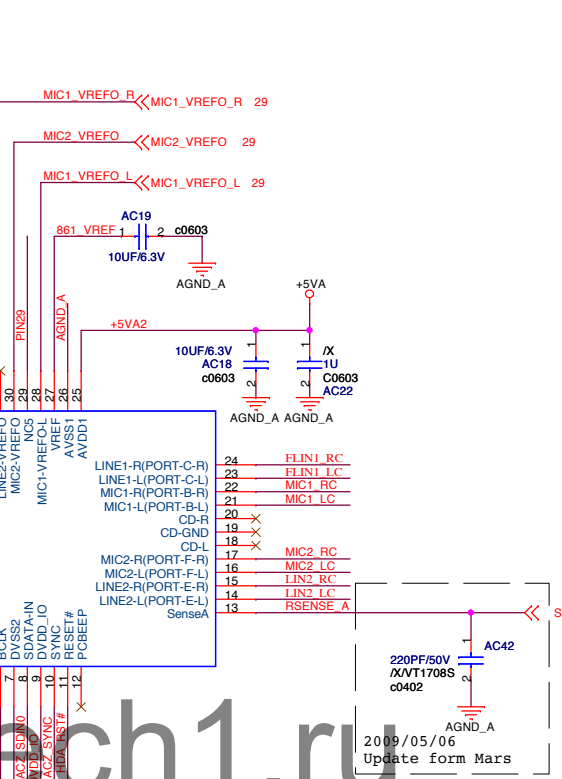
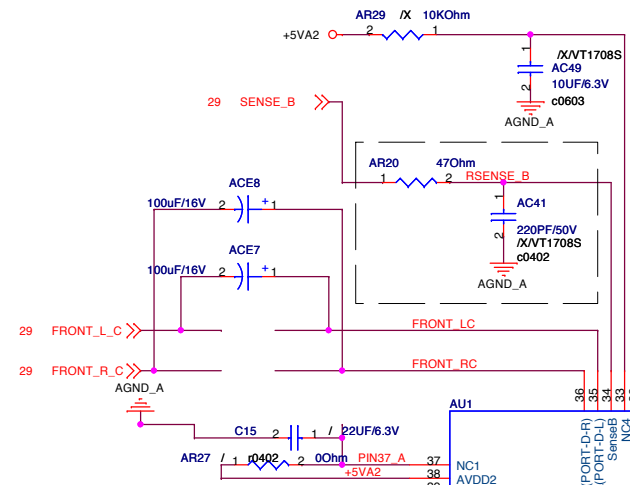
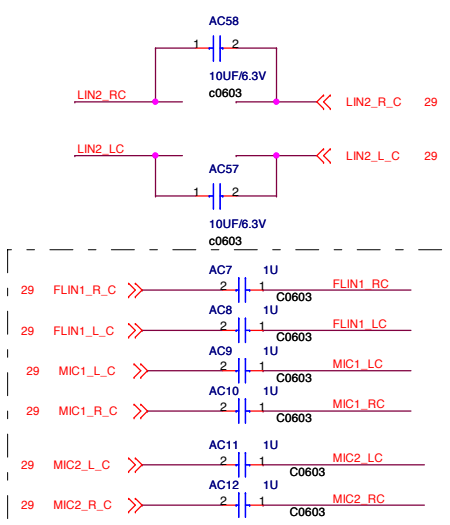




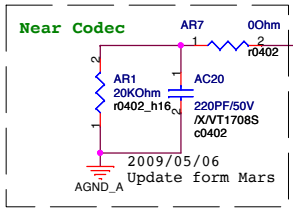
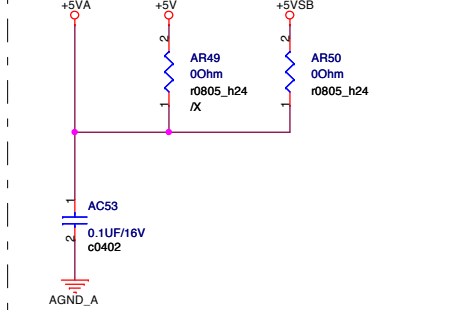
USB Power





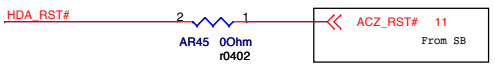
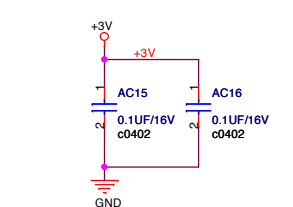
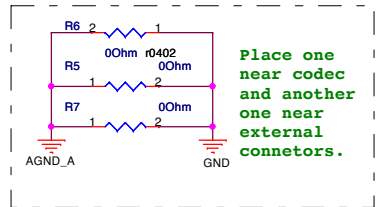
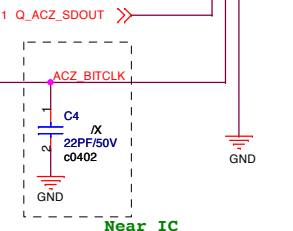
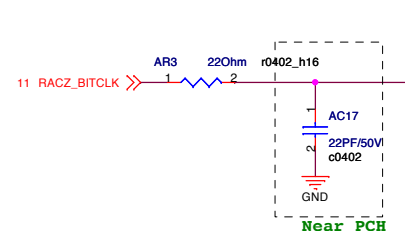
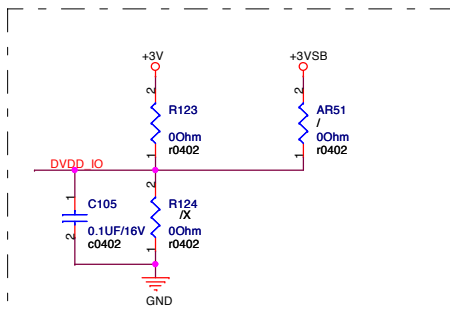
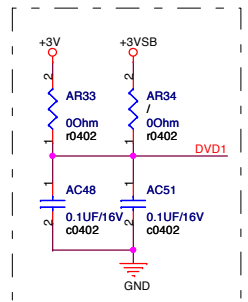
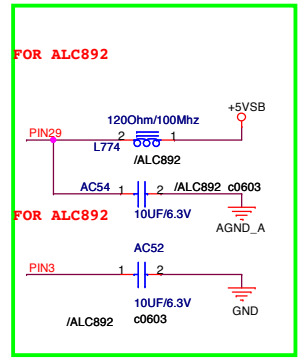


+5V Analog Power Switch

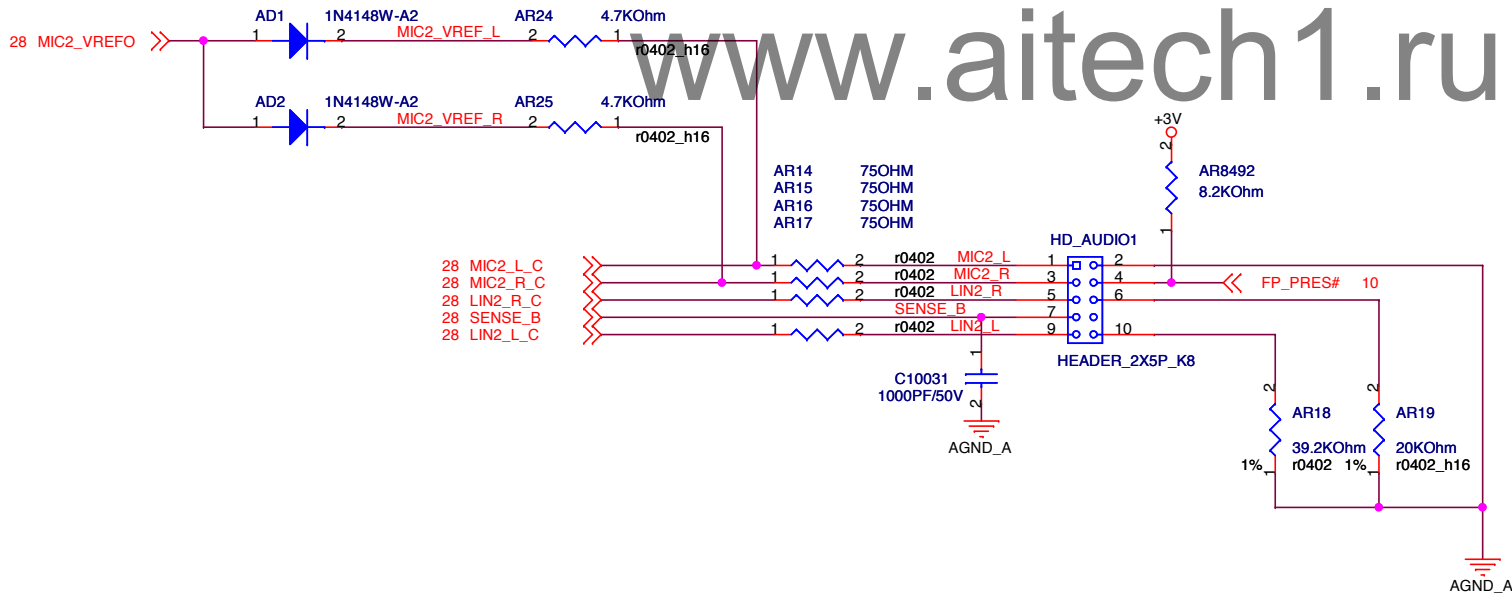
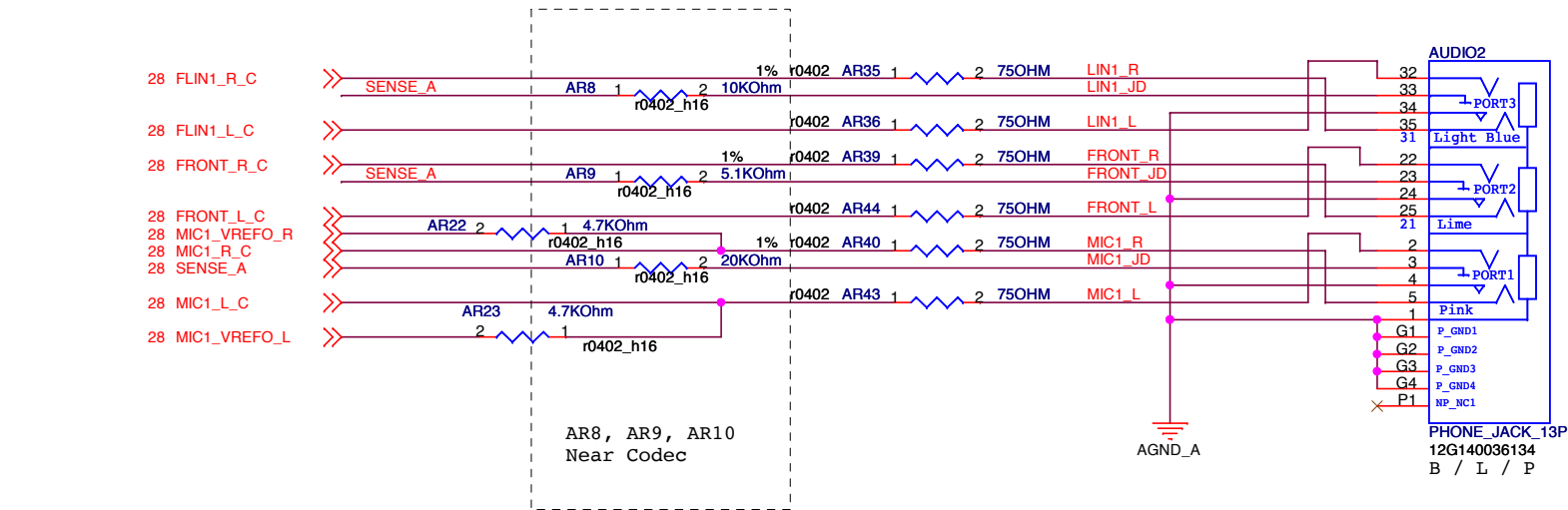


NOTE: ASUS symbol mistake
Pin45: SIDE_L
Pin46: SIDE_R

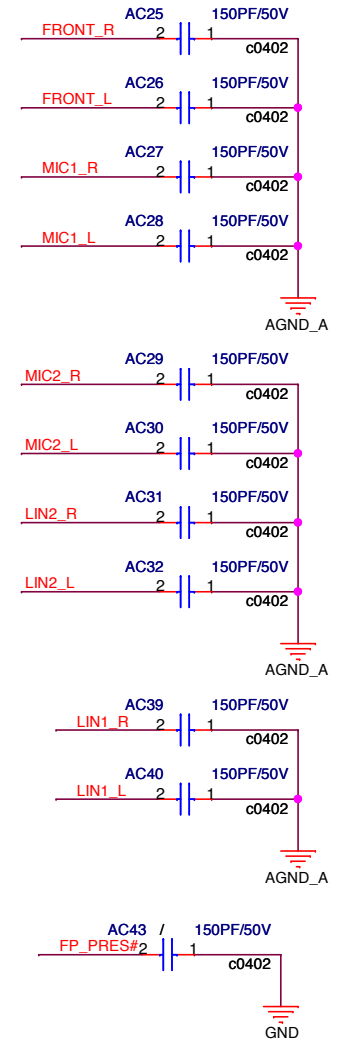
www.aitech1.ru



To support Intel HDMI Link, DVDD_IO change to +1.5V (Install R79, uninstall R123)



For EMI



B75M-DGS

ASRock		Title : ALC662 Codec_2	
ASRock Inc.		Engineer: Chia-wei Chang	
Size	Project Name	Rev	
Custom	B75M-DGS	2.00	
Date: Thursday, November 22, 2012		Sheet	of
		29	48

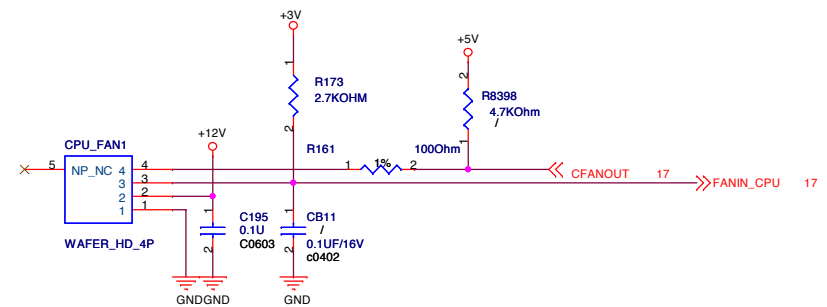
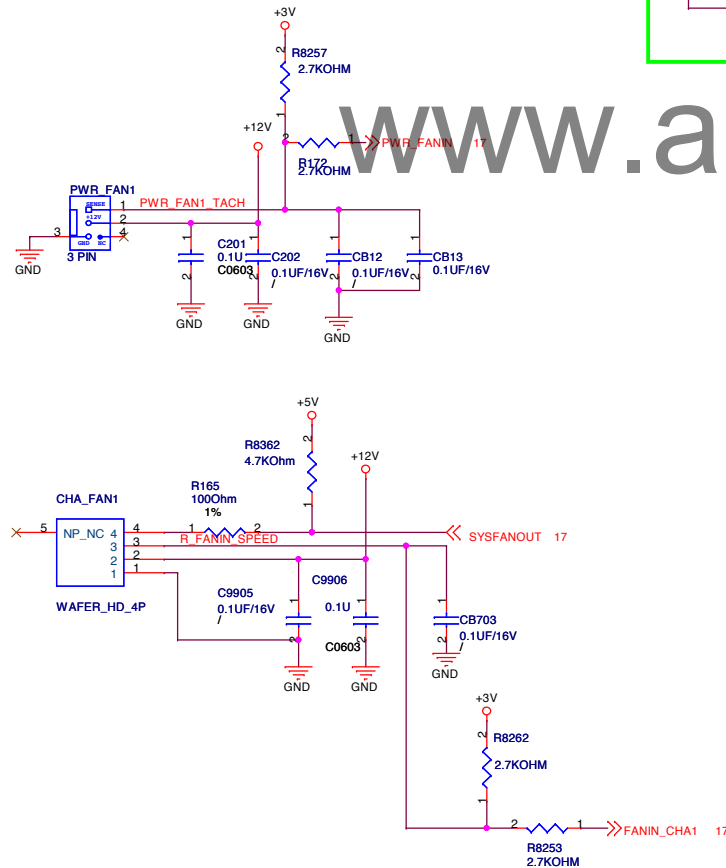
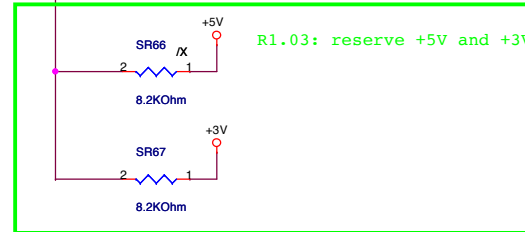
SMBus Switch

1.00 SMBus connect to two kind of devices, one use Main power, another use Standby power, so use this switch circuit to isolate those two device.
SMB_CLK and SMB_DATA for Standby device.
SMB_CLK_MAIN and SMB_DATA_MAIN for Main power device.

SMB_CLK and SMB_DATA connects to the ICH10R

Mount those SR64 and SR65 if we want to support PCI 2.3

SMB_CLK_PCI and SMB_DATA_PCI connects to the PCIE slot



B75M-DGS

ASRock		Title : SMBUS SWITCH,FAN	
ASRock Inc.		Engineer: Chia-wei Chang	
Size	Project Name	Rev	
A3	B75M-DGS	2.00	
Date: Thursday, November 22, 2012		Sheet	30 of 48

www.aitech1.ru

B75M-DGS

		Title : CPU FAN	
<small>ASRock Inc.</small>		Engineer: Chia-wei Chang	
Size	Project Name		Rev
A3	B75M-DGS		2.00
Date: Thursday, November 22, 2012		Sheet	31 of 48

+5V_DUAL_USB
circuit diagram

The diagram shows a purple wire connecting the +5V_DUAL pin to the +5V_DUAL_USB pin. The +5V_DUAL_USB pin is highlighted with a green rectangular box.

The schematic diagram illustrates the ATX power supply section of the board. It features the ATXPWR1 connector with pins 1 through 24. Key components include capacitors C9948, C26, C253, C254, C274, C300, C284, C286, C302, C285, and C299, all with values of 0.1uF/16V or 1uF/16V. A diode D10 (1N4148W-A2) is connected to the PWR_CON_24P pin. Resistor R204 (2.7k) is connected to the ATX+5VSB pin. The diagram also shows the connection of the ATX power rails: +5V, +3V, -12V, +12V, ATX+5VSB, and ATX+5VSB. A watermark 'www.digchip.com' is visible across the center of the diagram.

S3 circuit diagram

17.39 +3VSBWSW

17 PWROK_PS

5VSB

5VSB_GATE

5V_DUAL

5V

5V_GATE

5V_DUAL

Q5 2N7002K

Q6 MMBT3904R-DK

Q745 AP2309GN

Q744 AP72T02GH

Q8 PMBS3904

R185 00Ohm

R249 1K0Ohm /X

R186 8.2K0Ohm

R182 1K0Ohm

R184 1K0Ohm

R190 2.7K0Ohm

R192 10K0Ohm /X

R181 2.7K0Ohm

R188 00Ohm

R189 00Ohm

R191 00Ohm

R193 00Ohm

R194 00Ohm

R195 00Ohm

R196 00Ohm

R197 00Ohm

R198 00Ohm

R199 00Ohm

R200 00Ohm

R201 00Ohm

R202 00Ohm

R203 00Ohm

R204 00Ohm

R205 00Ohm

R206 00Ohm

R207 00Ohm

R208 00Ohm

R209 00Ohm

R210 00Ohm

R211 00Ohm

R212 00Ohm

R213 00Ohm

R214 00Ohm

R215 00Ohm

R216 00Ohm

R217 00Ohm

R218 00Ohm

R219 00Ohm

R220 00Ohm

R221 00Ohm

R222 00Ohm

R223 00Ohm

R224 00Ohm

R225 00Ohm

R226 00Ohm

R227 00Ohm

R228 00Ohm

R229 00Ohm

R230 00Ohm

R231 00Ohm

R232 00Ohm

R233 00Ohm

R234 00Ohm

R235 00Ohm

R236 00Ohm

R237 00Ohm

R238 00Ohm

R239 00Ohm

R240 00Ohm

R241 00Ohm

R242 00Ohm

R243 00Ohm

R244 00Ohm

R245 00Ohm

R246 00Ohm

R247 00Ohm

R248 00Ohm

R249 1K0Ohm /X

R250 00Ohm

R251 00Ohm

R252 00Ohm

R253 00Ohm

R254 00Ohm

R255 00Ohm

R256 00Ohm

R257 00Ohm

R258 00Ohm

R259 00Ohm

R260 00Ohm

R261 00Ohm

R262 00Ohm

R263 00Ohm

R264 00Ohm

R265 00Ohm

R266 00Ohm

R267 00Ohm

R268 00Ohm

R269 00Ohm

R270 00Ohm

R271 00Ohm

R272 00Ohm

R273 00Ohm

R274 00Ohm

R275 00Ohm

R276 00Ohm

R277 00Ohm

R278 00Ohm

R279 00Ohm

R280 00Ohm

R281 00Ohm

R282 00Ohm

R283 00Ohm

R284 00Ohm

R285 00Ohm

R286 00Ohm

R287 00Ohm

R288 00Ohm

R289 00Ohm

R290 00Ohm

R291 00Ohm

R292 00Ohm

R293 00Ohm

R294 00Ohm

R295 00Ohm

R296 00Ohm

R297 00Ohm

R298 00Ohm

R299 00Ohm

R300 00Ohm

R301 00Ohm

R302 00Ohm

R303 00Ohm

R304 00Ohm

R305 00Ohm

R306 00Ohm

R307 00Ohm

R308 00Ohm

R309 00Ohm

R310 00Ohm

R311 00Ohm

R312 00Ohm

R313 00Ohm

R314 00Ohm

R315 00Ohm

R316 00Ohm

R317 00Ohm

R318 00Ohm

R319 00Ohm

R320 00Ohm

R321 00Ohm

R322 00Ohm

R323 00Ohm

R324 00Ohm

R325 00Ohm

R326 00Ohm

R327 00Ohm

R328 00Ohm

R329 00Ohm

R330 00Ohm

R331 00Ohm

R332 00Ohm

R333 00Ohm

R334 00Ohm

R335 00Ohm

R336 00Ohm

R337 00Ohm

R338 00Ohm

R339 00Ohm

R340 00Ohm

R341 00Ohm

R342 00Ohm

R343 00Ohm

R344 00Ohm

R345 00Ohm

R346 00Ohm

R347 00Ohm

R348 00Ohm

R349 00Ohm

R350 00Ohm

R351 00Ohm

R352 00Ohm

R353 00Ohm

R354 00Ohm

R355 00Ohm

R356 00Ohm

R357 00Ohm

R358 00Ohm

R359 00Ohm

R360 00Ohm

R361 00Ohm

R362 00Ohm

R363 00Ohm

R364 00Ohm

R365 00Ohm

R366 00Ohm

R367 00Ohm

R368 00Ohm

R369 00Ohm

R370 00Ohm

R371 00Ohm

R372 00Ohm

R373 00Ohm

R374 00Ohm

R375 00Ohm

R376 00Ohm

R377 00Ohm

R378 00Ohm

R379 00Ohm

R380 00Ohm

R381 00Ohm

R382 00Ohm

R383 00Ohm

R384 00Ohm

R385 00Ohm

R386 00Ohm

R387 00Ohm

R388 00Ohm

R389 00Ohm

R390 00Ohm

R391 00Ohm

R392 00Ohm

R393 00Ohm

R394 00Ohm

R395 00Ohm

R396 00Ohm

R397 00Ohm

R398 00Ohm

R399 00Ohm

R400 00Ohm

R401 00Ohm

R402 00Ohm

R403 00Ohm

R404 00Ohm

R405 00Ohm

R406 00Ohm

R407 00Ohm

R408 00Ohm

R409 00Ohm

R410 00Ohm

R411 00Ohm

R412 00Ohm

R413 00Ohm

R414 00Ohm

R415 00Ohm

R416 00Ohm

R417 00Ohm

R418 00Ohm

R419 00Ohm

R420 00Ohm

R421 00Ohm

R422 00Ohm

R423 00Ohm

R424 00Ohm

R425 00Ohm

R426 00Ohm

R427 00Ohm

R428 00Ohm

R429 00Ohm

R430 00Ohm

R431 00Ohm

R432 00Ohm

R433 00Ohm

R434 00Ohm

R435 00Ohm

R436 00Ohm

R437 00Ohm

R438 00Ohm

R439 00Ohm

R440 00Ohm

R441 00Ohm

R442 00Ohm

R443 00Ohm

R444 00Ohm

R445 00Ohm

R446 00Ohm

R447 00Ohm

R448 00Ohm

R449 00Ohm

R450 00Ohm

R451 00Ohm

R452 00Ohm

R453 00Ohm

R454 00Ohm

R455 00Ohm

R456 00Ohm

R457 00Ohm

R458 00Ohm

R459 00Ohm

R460 00Ohm

R461 00Ohm

R462 00Ohm

R463 00Ohm

R464 00Ohm

R465 00Ohm

R466 00Ohm

R467 00Ohm

R468 00Ohm

R469 00Ohm

R470 00Ohm

R471 00Ohm

R472 00Ohm

R473 00Ohm

R474 00Ohm

R475 00Ohm

R476 00Ohm

R477 00Ohm

R478 00Ohm

R479 00Ohm

R480 00Ohm

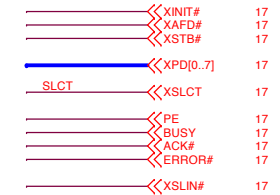
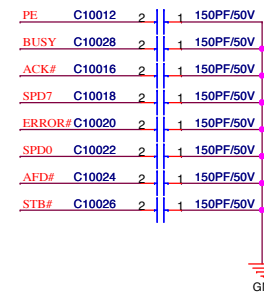
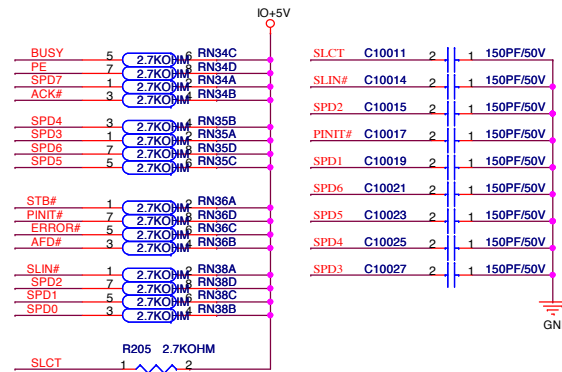
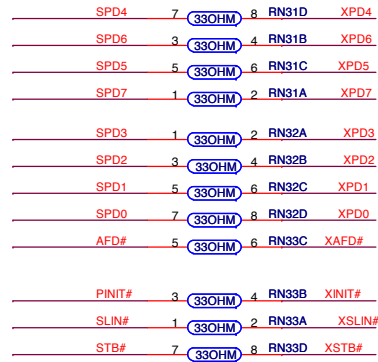
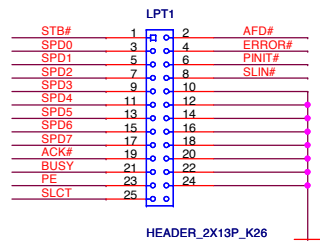
R481 00Ohm

R482 00Ohm

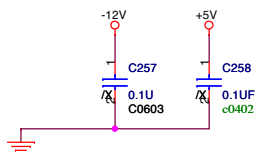
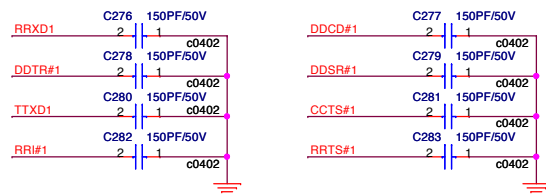
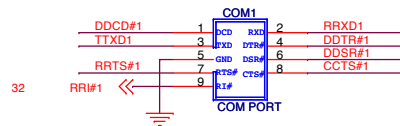
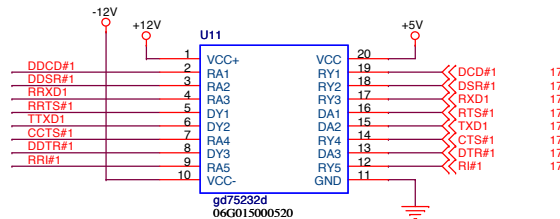
B75M-DGS

		Title : POK_DUALSW_ENASUS	
ASRock Inc.		Engineer: Chia-wei Chang	
Size A3	Project Name B75M-DGS	Rev 2.00	
Date: Tuesday, December 11, 2012		Sheet 32	of 48

Parallel Port

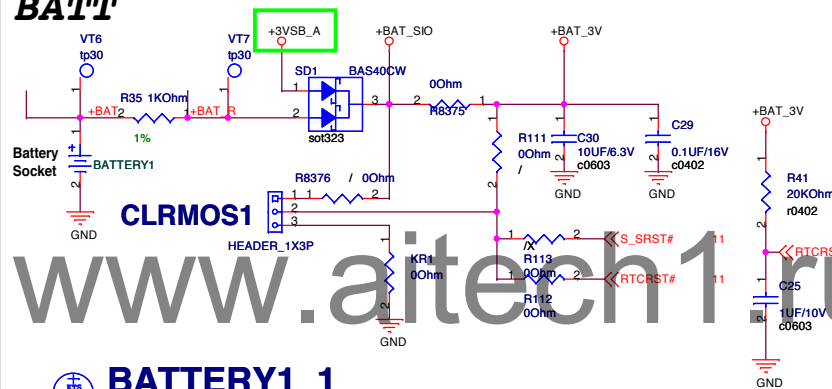


COM



BATT

```
prevent using battery in deep s4/s5 mode.
```

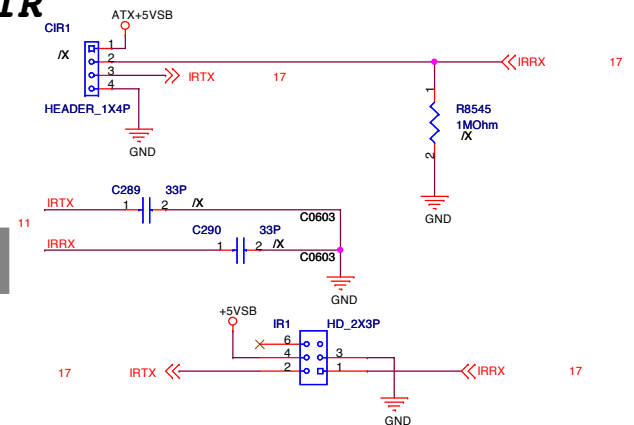
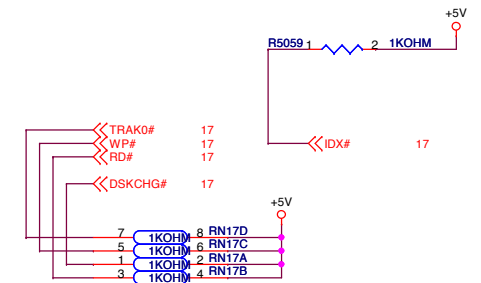


BATTERY1_1

3V/220mAh

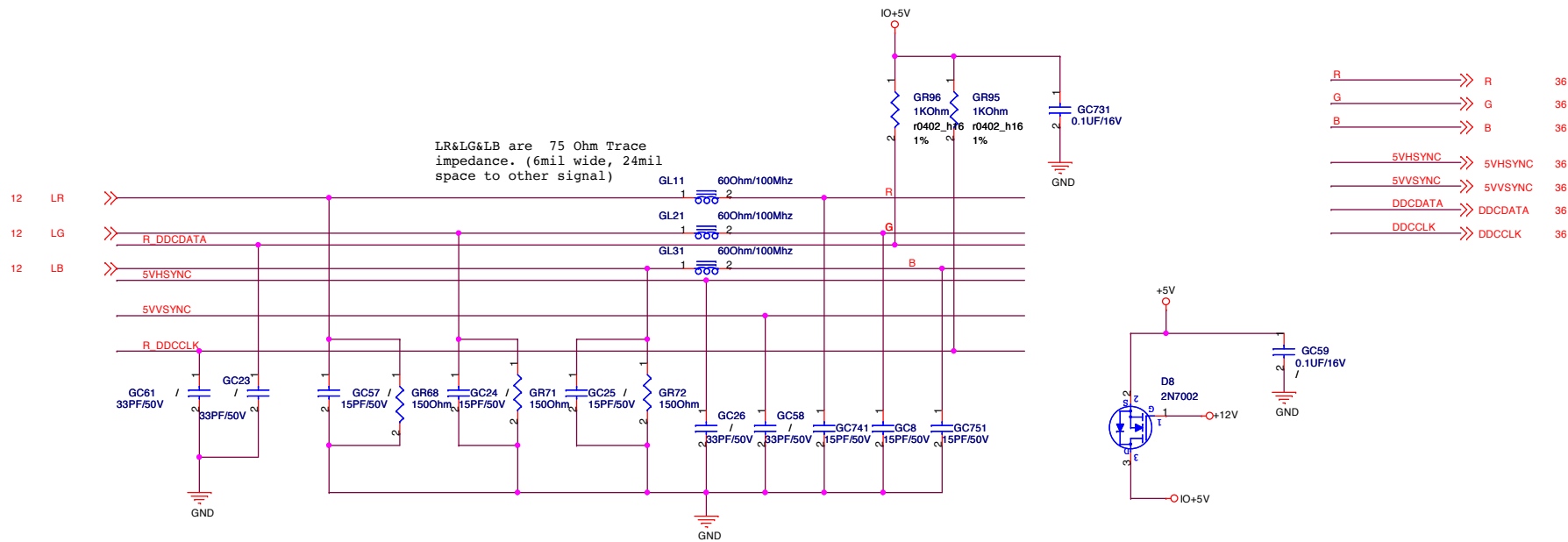


IR

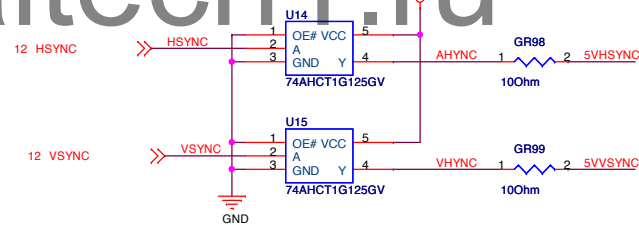
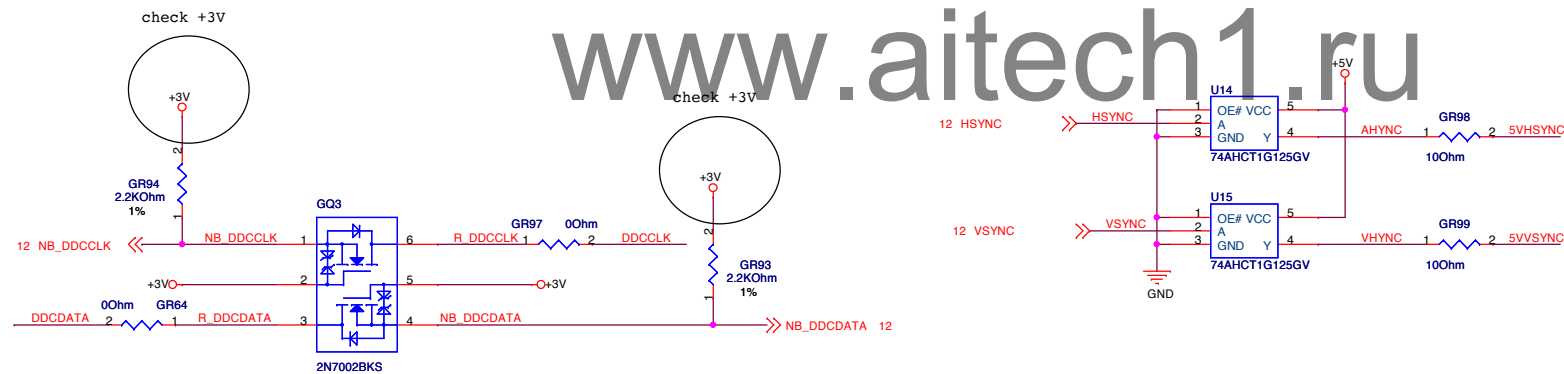
***TPM***

B75M-DGS



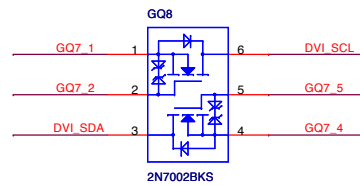
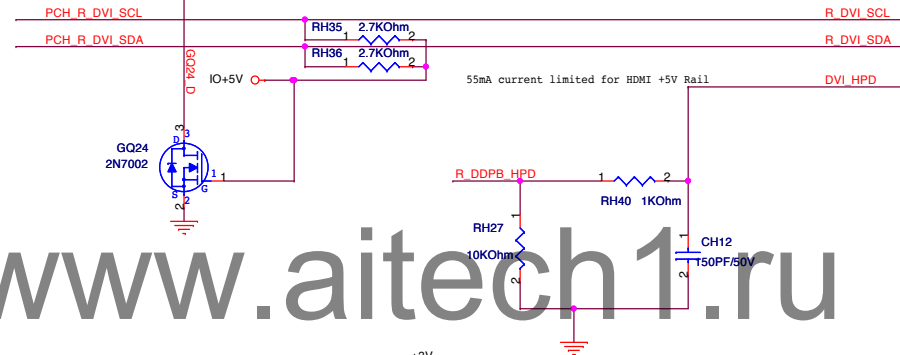
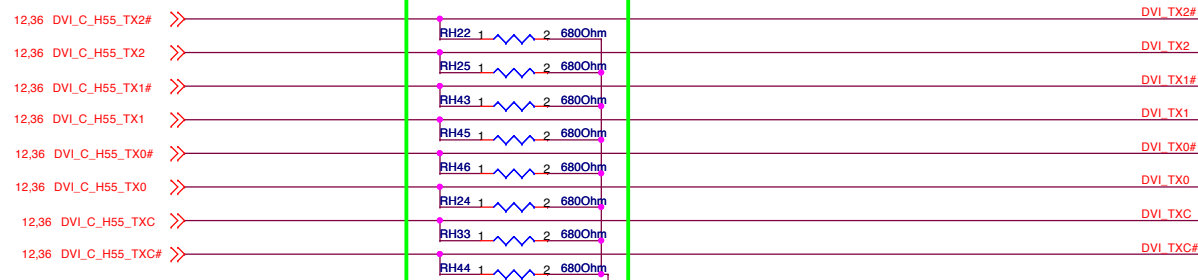


R 36
G 36
B 36
5VHSYNC 36
5VVSYSNC 36
DDCDATA 36
DDCCLK 36

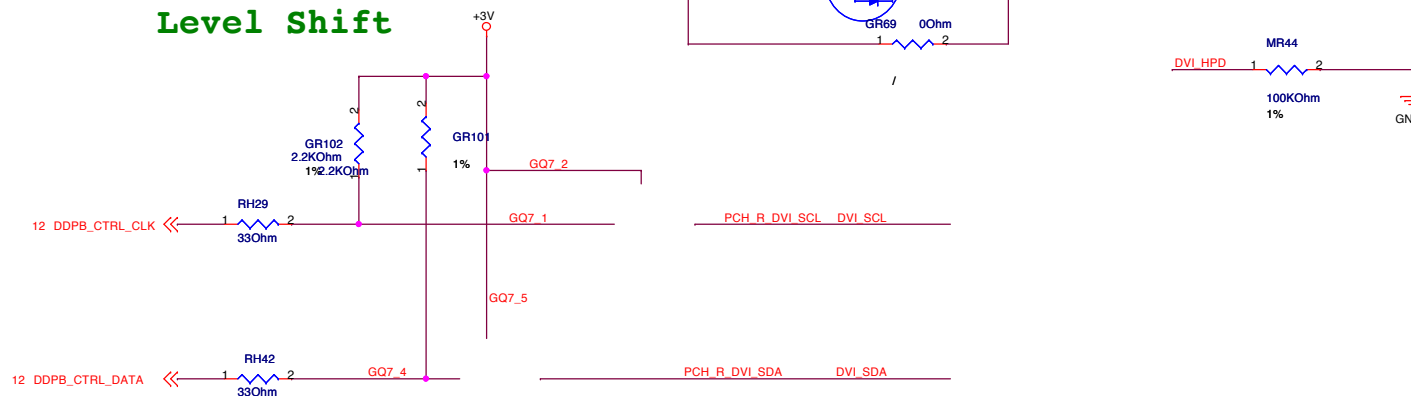


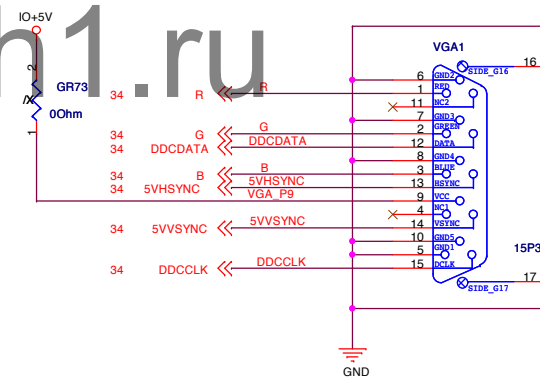
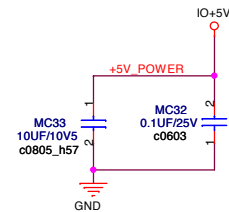
DVI CONNECTOR

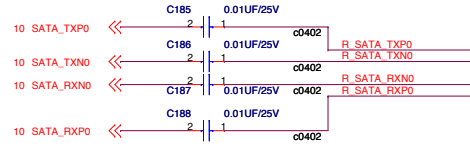
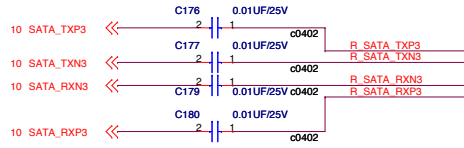
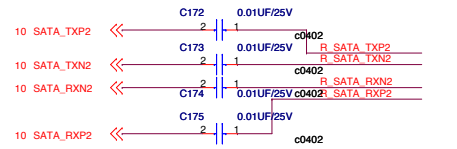
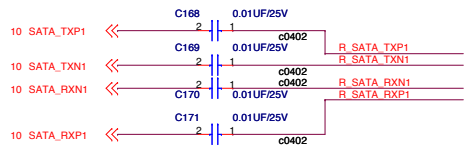
BOM爲1%



Level Shift

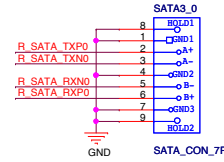




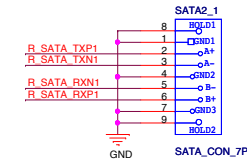
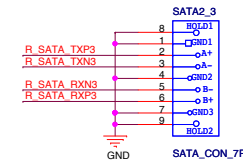
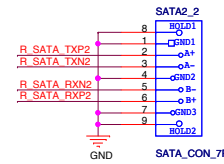


INTEL SATA3

Check SATA Port Name with leaders!!!



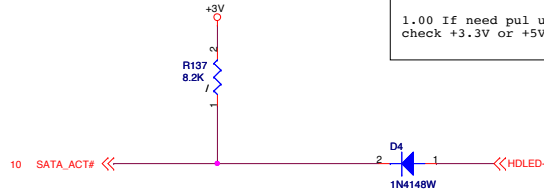
INTEL SATA2



SATA3 & SATA LED

1.00 Internal Pull UP

1.00 If need pul up,
check +3.3V or +5V

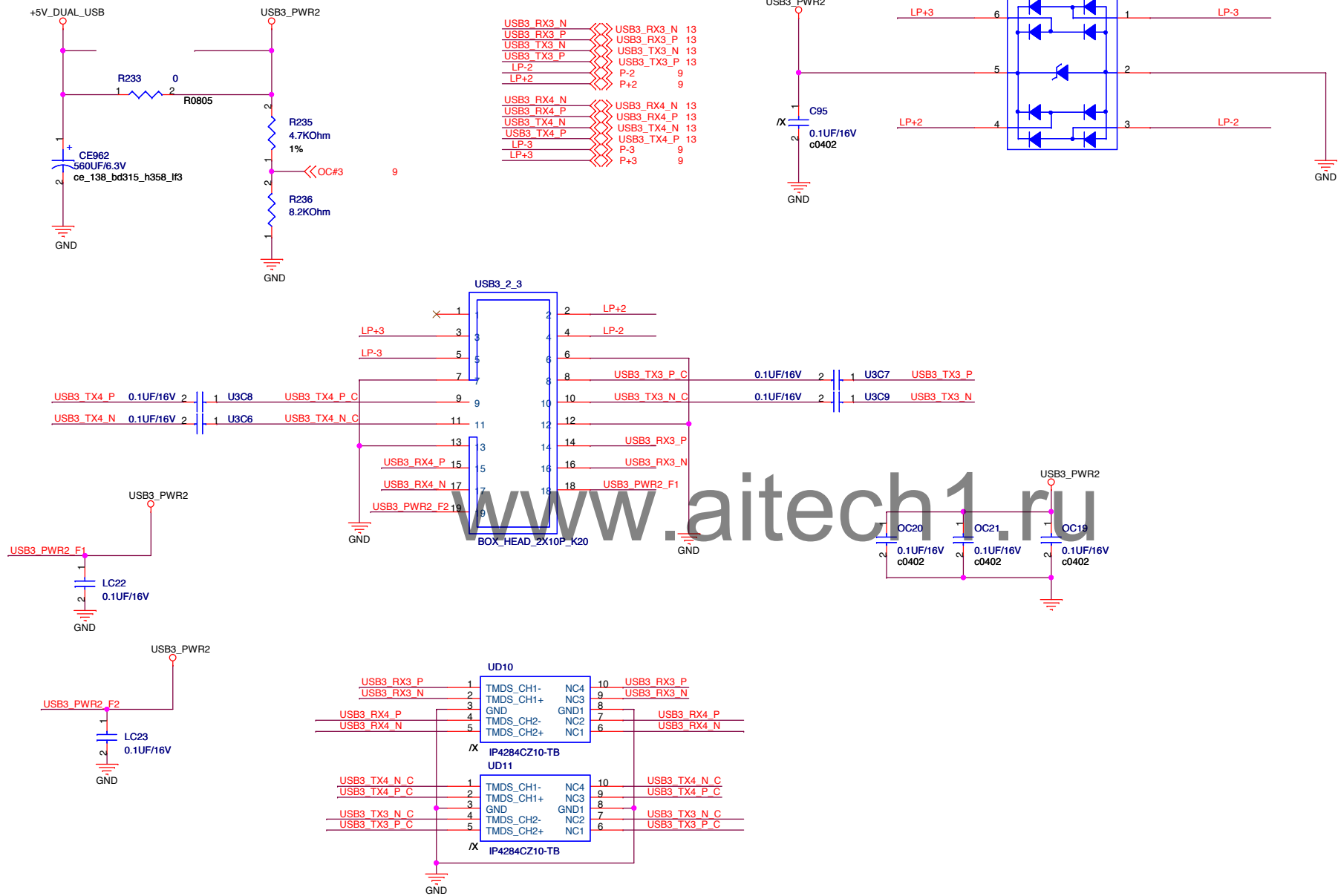


www.aitech1.ru

B75M-DGS

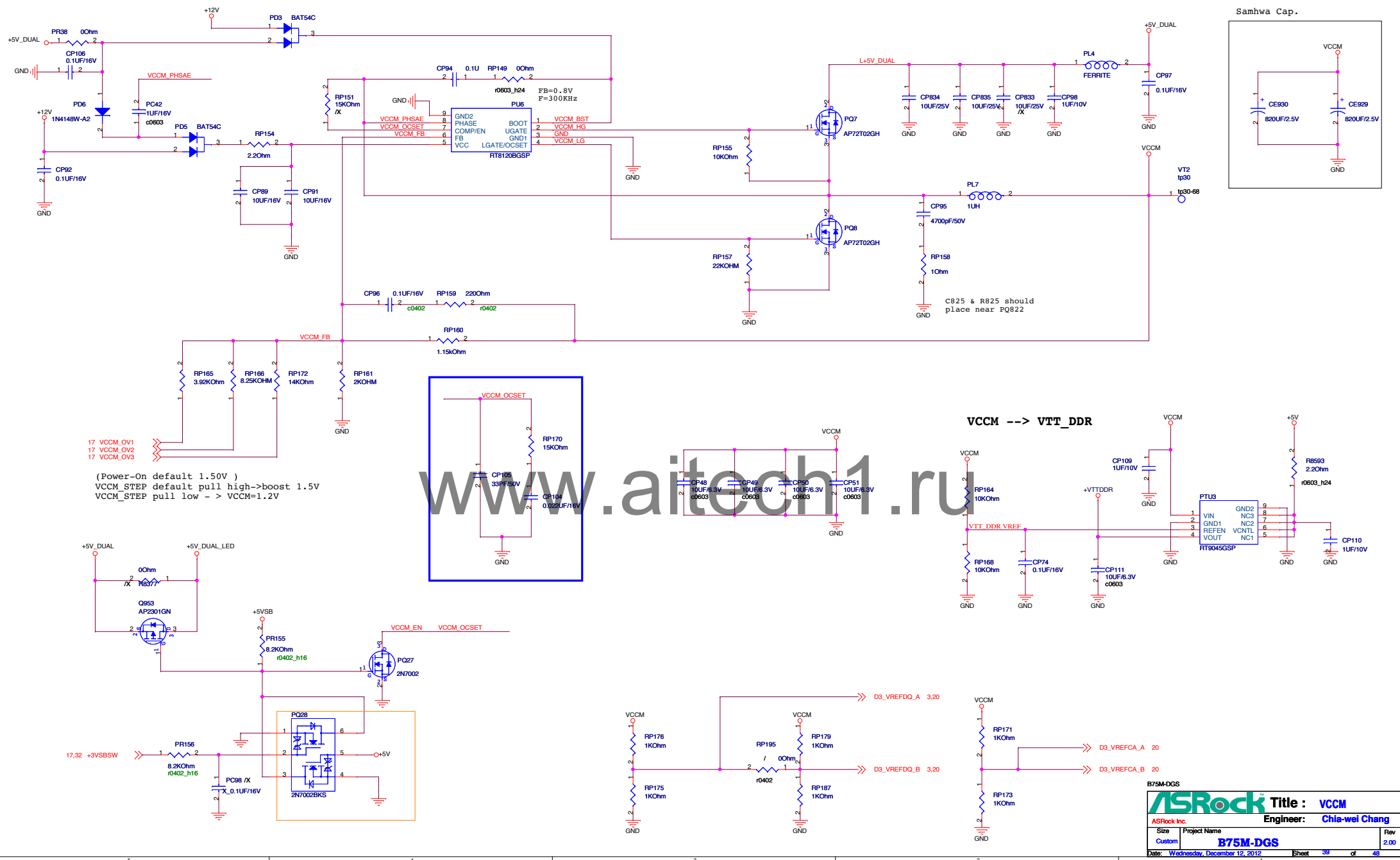
ASRock		Title : SATA3/SATA2 / ESATA	
ASRock Inc.		Engineer: Chia-wei Chang	
Size	Project Name	Rev	
Custom	B75M-DGS	2.00	
Date: Tuesday, December 11, 2012	Sheet 37	of 48	

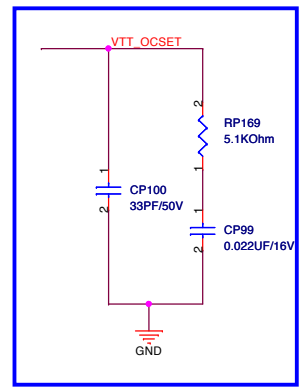
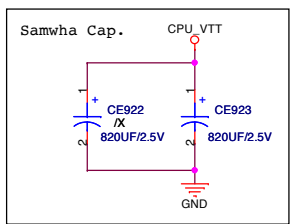
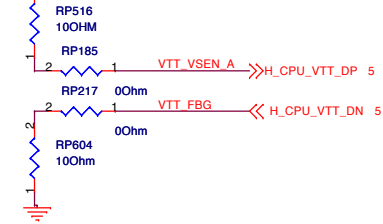
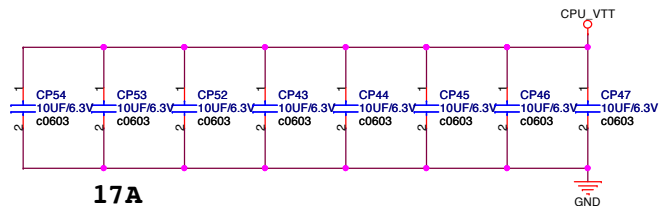
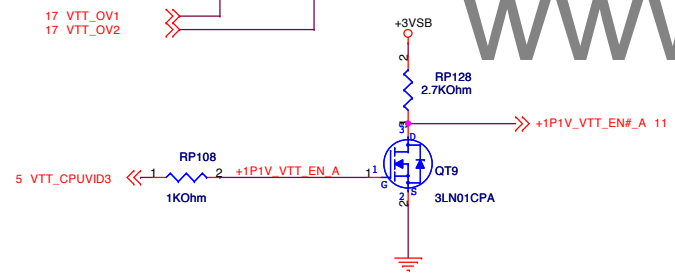
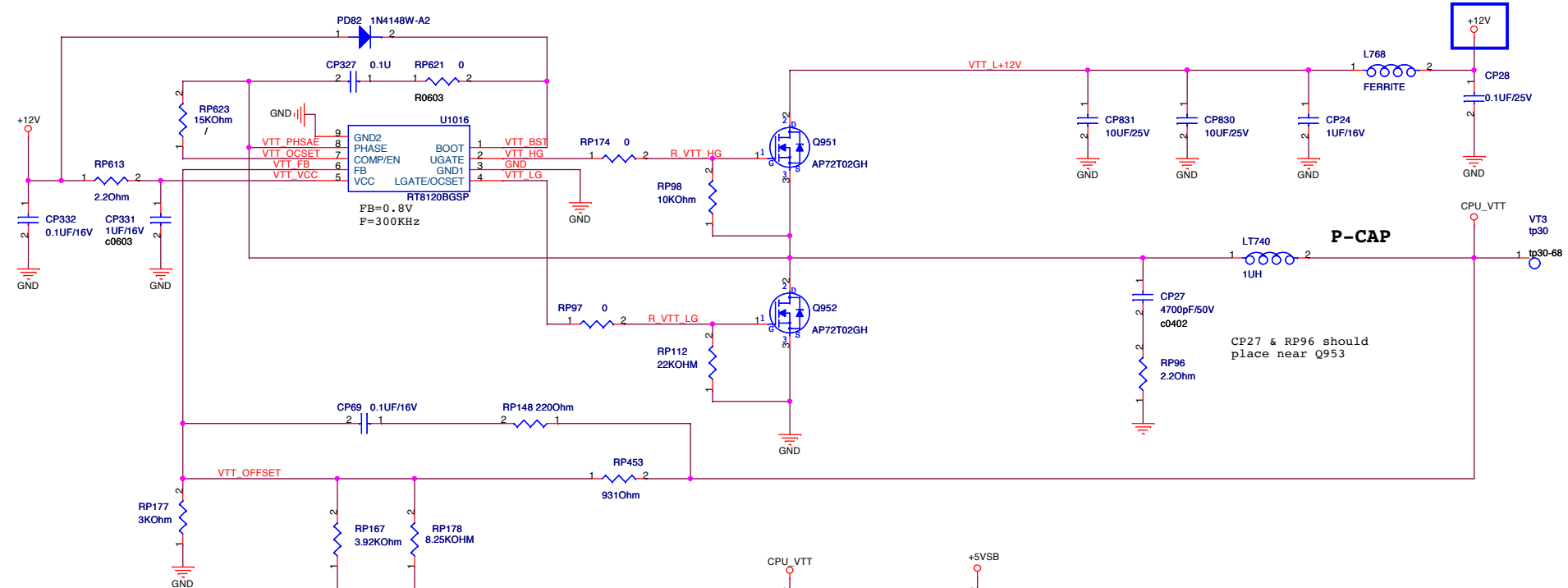
USB3_ 2_3

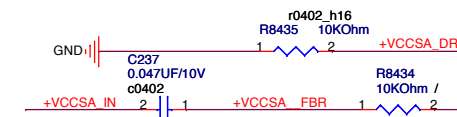
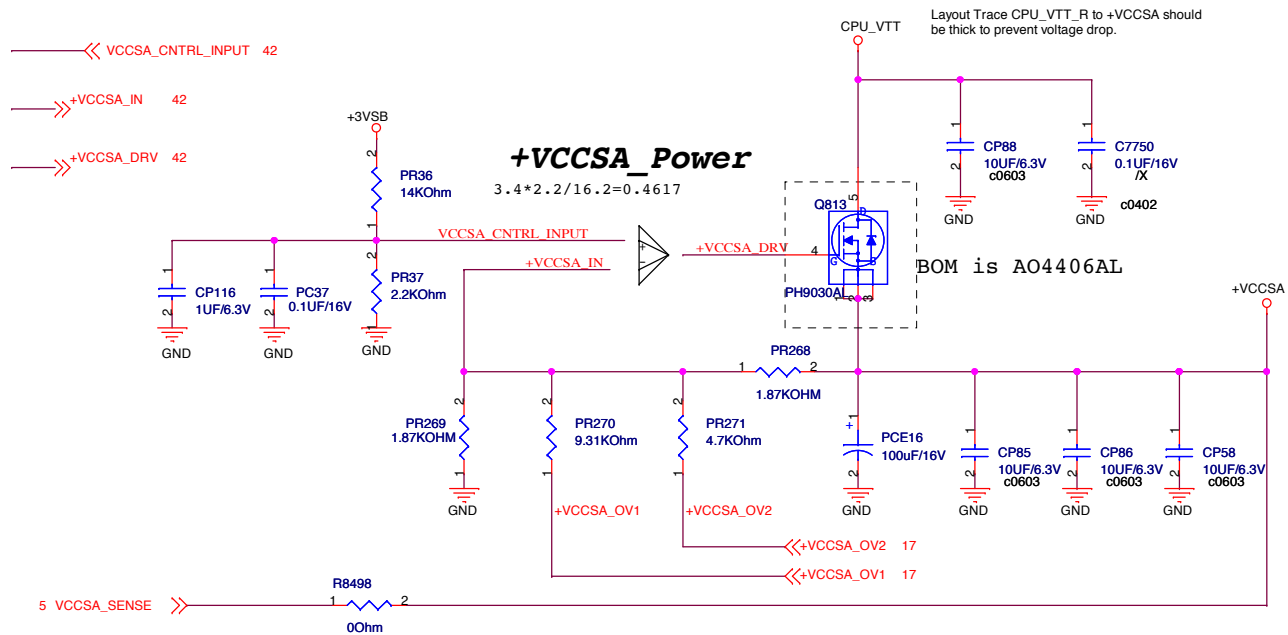


B75 Pro3-M

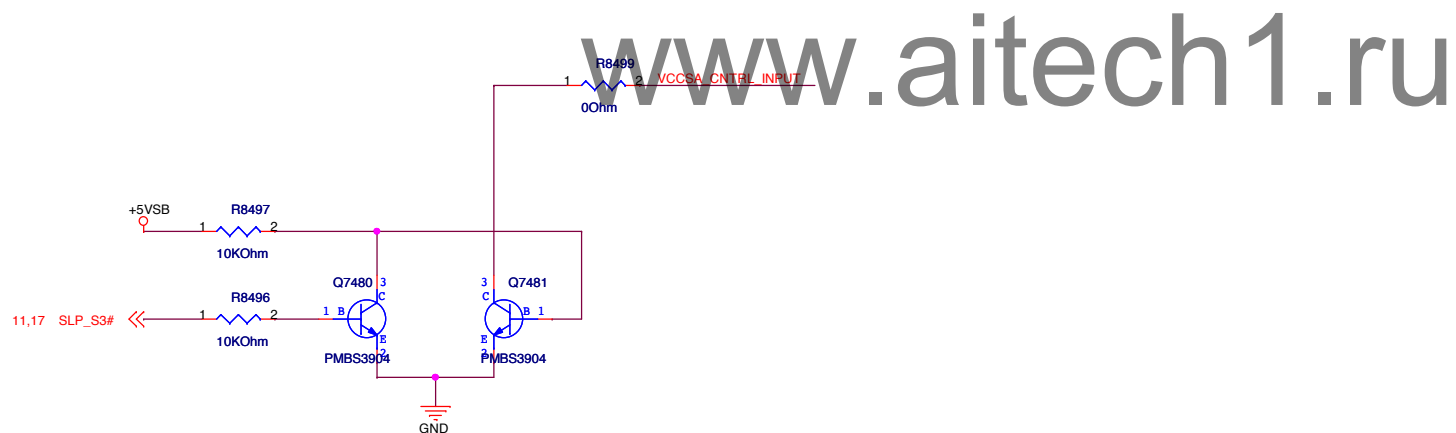
ASRock		Title : Front USB3	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size	Project Name	Rev	
Custom	B75 Pro3-M	2.00	
Date: Tuesday, December 11, 2012		Sheet	38 of 48







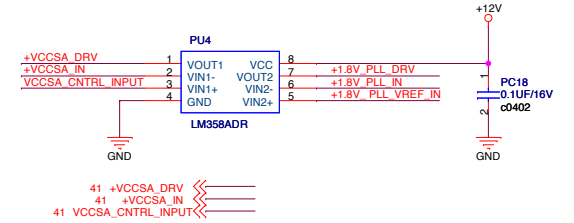
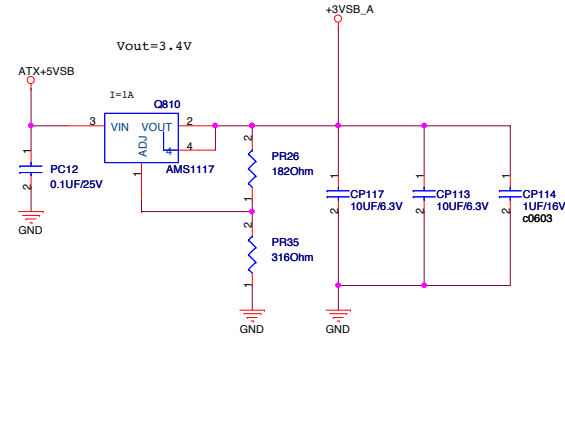
+VCCSA	OV1	OV2	
0.925V	H	H	(default)
1.016V	H	L	
1.107V	L	H	
1.200V	L	L	



B75M-DGS

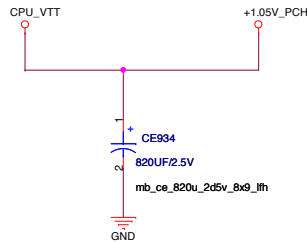
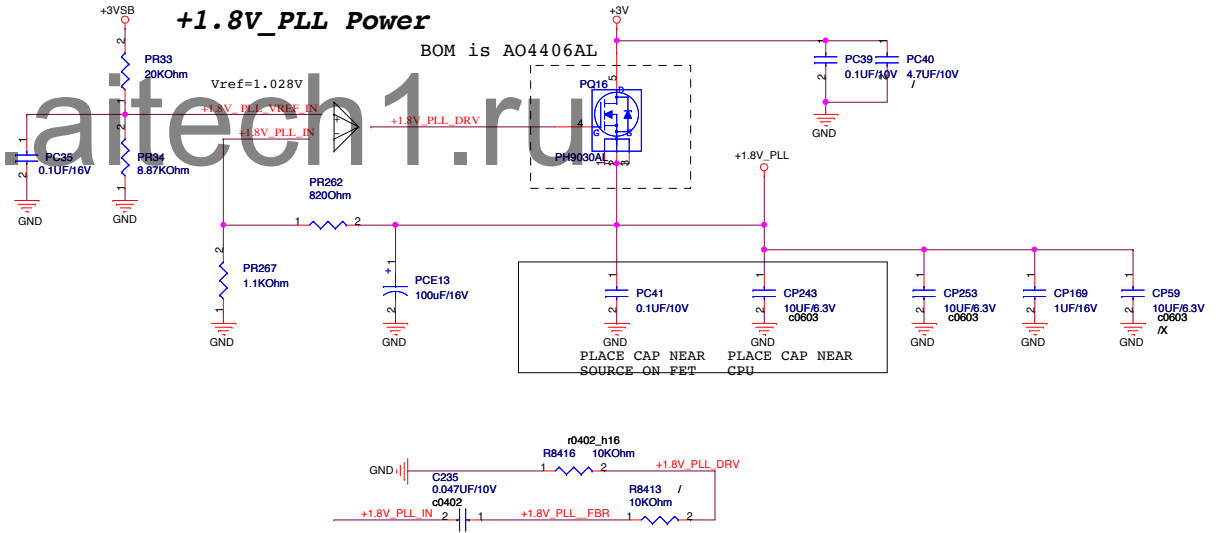
ASRock		Title : VSA	
ASRock Inc.		Engineer: Chia-wei Chang	
Size B	Project Name B75M-DGS		Rev 2.00
Date: Thursday, November 22, 2012		Sheet 41	of 48

+3VSB_A



+1.8V_PLL Power

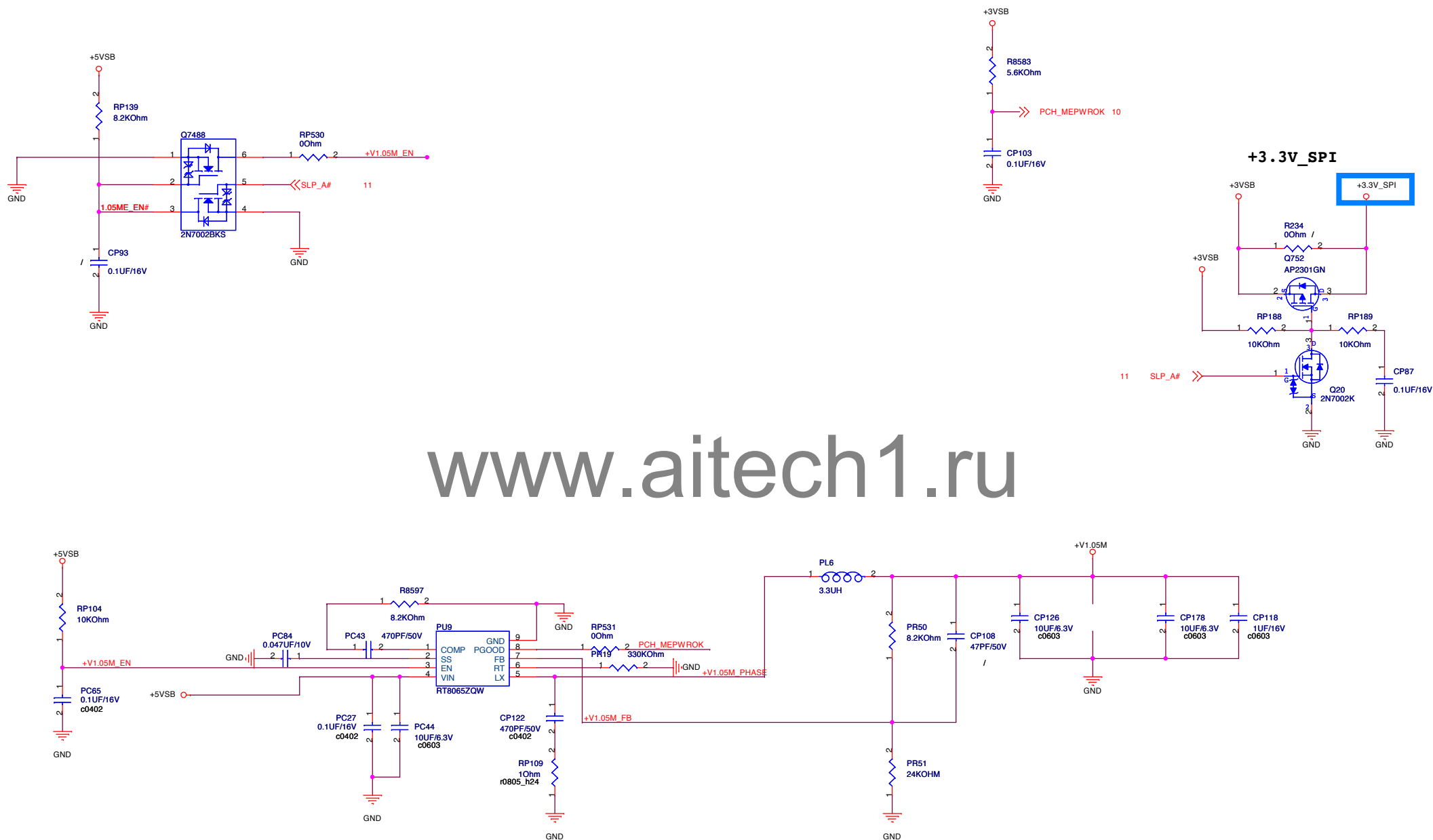
BOM is AO4406AL



B75M-DGS

ASRock Inc.		Title : DC to DC	
Engineer: Chia-wei Chang			
Size	Project Name		Rev
Custom	B75M-DGS		2.00
Date: Tuesday, November 27, 2012		Sheet 42	of 48


www.aitech1.ru



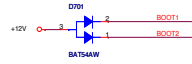
B75M-DGS

ASRock Title : ME Power	
ASRock Inc. Engineer: Chia-wei Chang	
Size A3	Project Name
Date: Tuesday, November 27, 2012	Sheet 43 of 48
Rev 2.00	

www.aitech1.ru

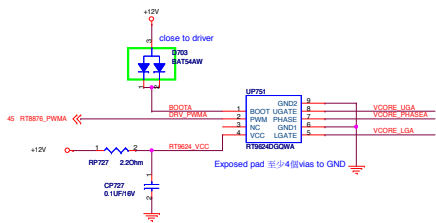
		Title : Voltage_Switch	
ASRock Inc.		Engineer: Chia-wei Chang	
Size	Project Name		Rev
B	B75M-DGS		2.00
Date: Thursday, November 22, 2012		Sheet 44	of 48

45 BOOT1 << BOOT1
45 VCORE_UG1 << VCORE_UG1
45 VCORE_PHASE1 << VCORE_PHASE1
45 VCORE_LG1 << VCORE_LG1



45 BOOT2 << BOOT2
45 VCORE_UG2 << VCORE_UG2
45 VCORE_PHASE2 << VCORE_PHASE2
45 VCORE_LG2 << VCORE_LG2

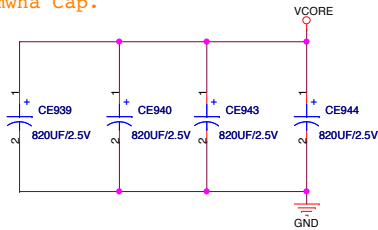
45 BOOT3 << BOOT3
45 VCORE_UG3 << VCORE_UG3
45 VCORE_PHASE3 << VCORE_PHASE3
45 VCORE_LG3 << VCORE_LG3



www.aitech1.ru

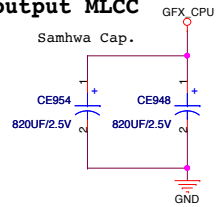
Vcore output P-CAP

Samwha Cap.

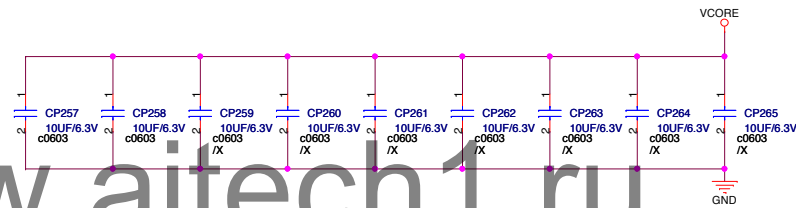
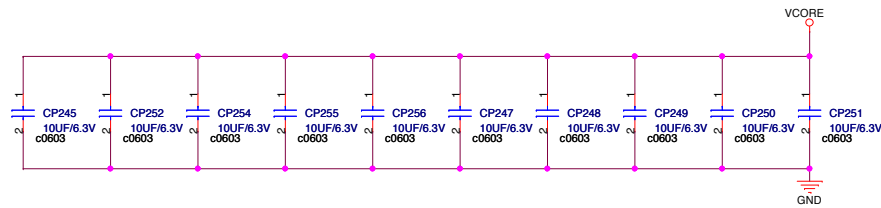
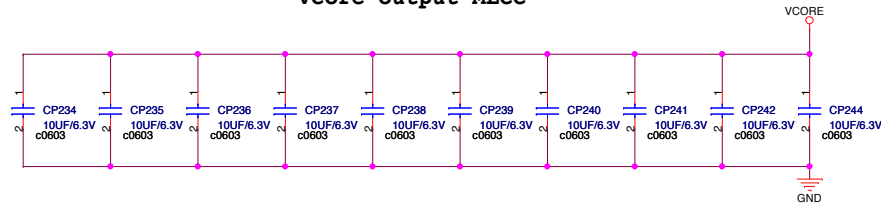


GFX output MLCC

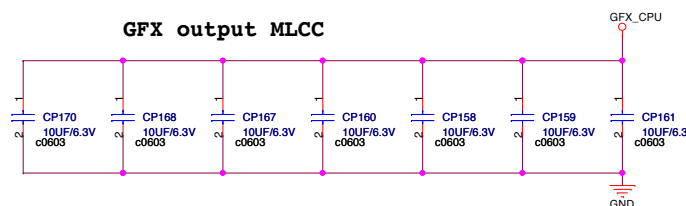
Samwha Cap.



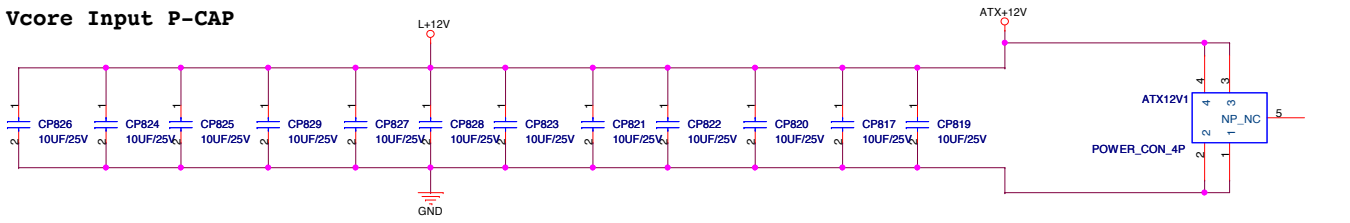
Vcore output MLCC



GFX output MLCC



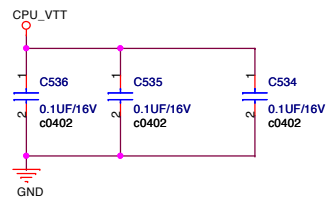
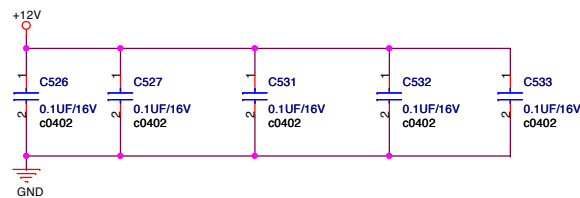
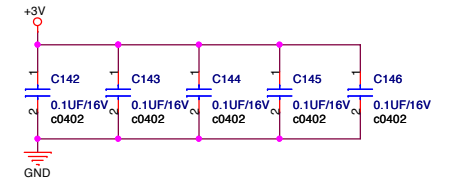
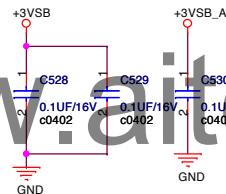
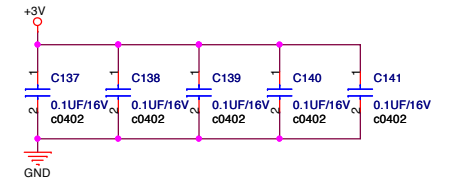
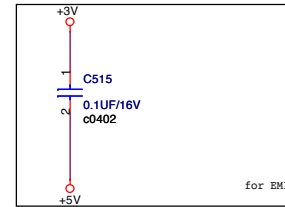
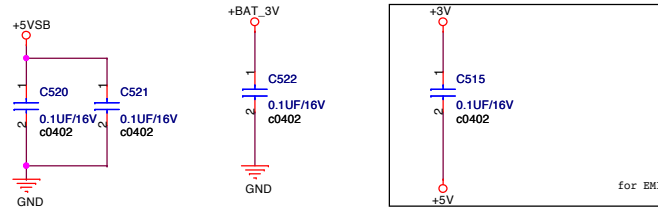
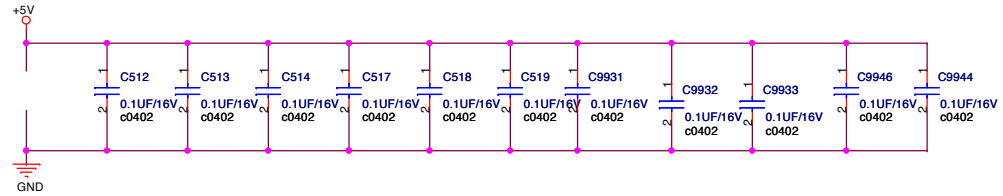
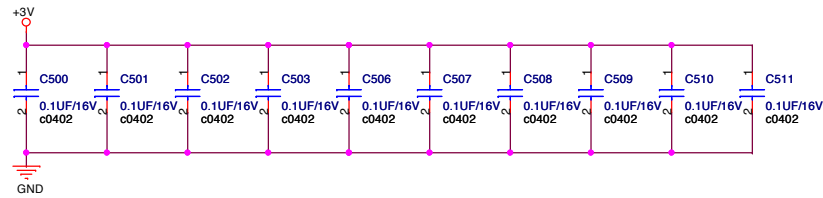
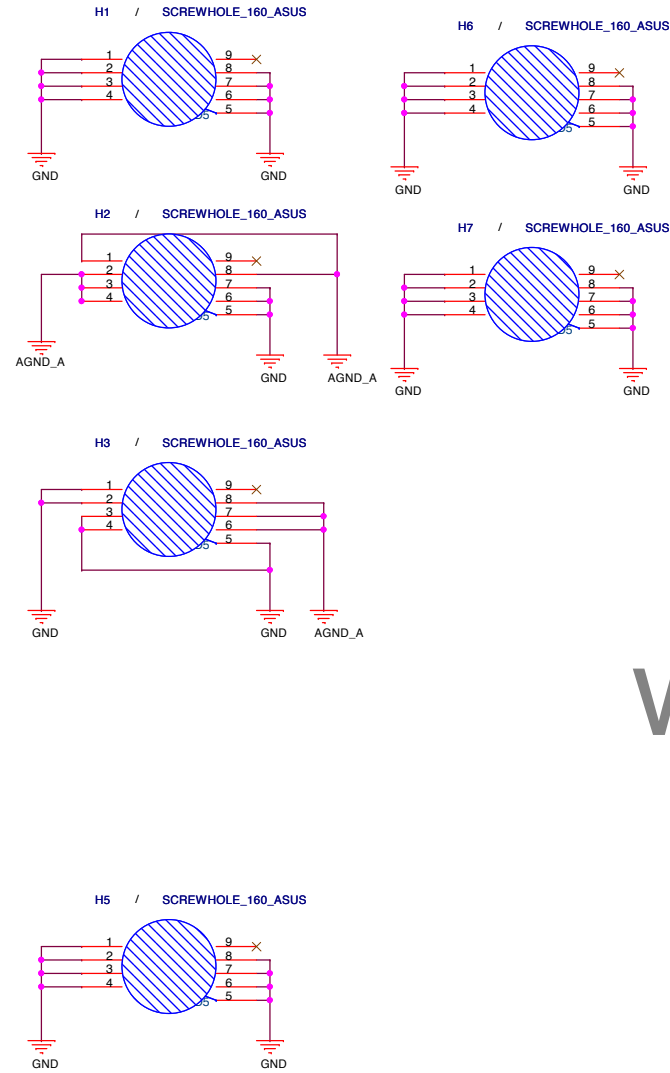
Vcore Input P-CAP



B75M-DGS

ASRock		Title : CPU CAP & Offset	
ASRock Inc.		Engineer: Chia-wei Chang	
Size	Project Name	Rev	
Custom	B75M-DGS	2.00	
Date: Wednesday, November 28, 2012	Sheet 47	of 48	

SCREW_HOLE



www.aitech1.ru